# JVC

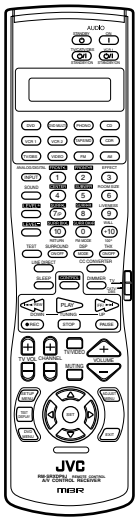
# SERVICE MANUAL

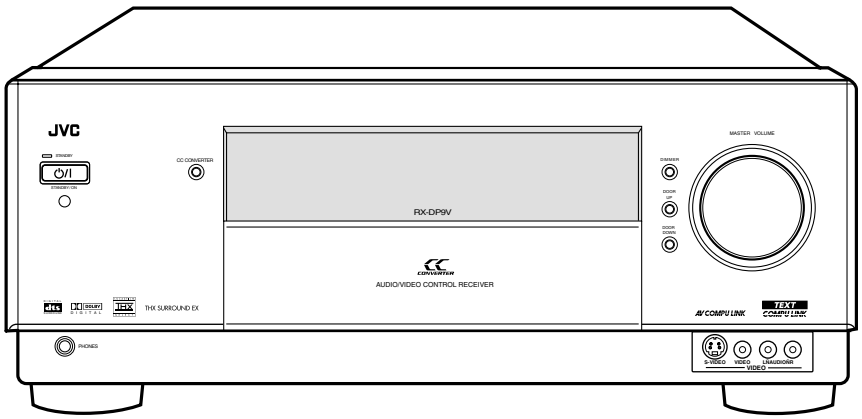
## AUDIO/VIDEO CONTROL RECEIVER

# RX-DP9VBK
# RX-DP9VSL

**Area Suffix**

J ---------- U.S.A.
C ---------- Canada






CONVERTER
TEXT COMPU LINK
DIGITAL dts SURROUND
DOLBY DIGITAL
LUCASFILM THX SELECT

AV COMPU LINK THX SURROUND EX

| Model | Color |
|---|---|
| RX-DP9VBK | Black |
| RX-DP9VSL | Silver |

## Contents

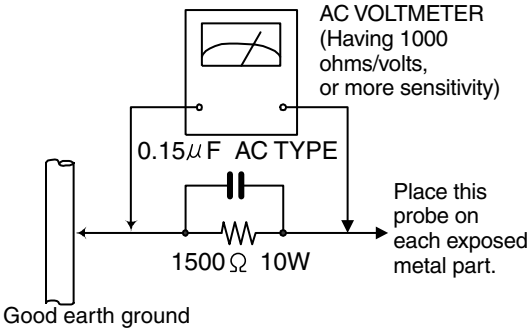




No.21019
Sep. 2001

## Safety Precautions

1. This design of this product contains special hardware and many circuits and components specially for safety purposes. For continued protection, no changes should be made to the original design unless authorized in writing by the manufacturer. Replacement parts must be identical to those used in the original circuits. Services should be performed by qualified personnel only.
2. Alterations of the design or circuitry of the product should not be made. Any design alterations of the product should not be made. Any design alterations or additions will void the manufacturer's warranty and will further relieve the manufacture of responsibility for personal injury or property damage resulting therefrom.
3. Many electrical and mechanical parts in the products have special safety-related characteristics. These characteristics are often not evident from visual inspection nor can the protection afforded by them necessarily be obtained by using replacement components rated for higher voltage, wattage, etc. Replacement parts which have these special safety characteristics are identified in the Parts List of Service Manual. Electrical components having such features are identified by shading on the schematics and by (⚠) on the Parts List in the Service Manual. The use of a substitute replacement which does not have the same safety characteristics as the recommended replacement parts shown in the Parts List of Service Manual may create shock, fire, or other hazards.
4. The leads in the products are routed and dressed with ties, clamps, tubings, barriers and the like to be separated from live parts, high temperature parts, moving parts and/or sharp edges for the prevention of electric shock and fire hazard. When service is required, the original lead routing and dress should be observed, and it should be confirmed that they have been returned to normal, after re-assembling.
5. Leakage current check (Electrical shock hazard testing)
   After re-assembling the product, always perform an isolation check on the exposed metal parts of the product (antenna terminals, knobs, metal cabinet, screw heads, headphone jack, control shafts, etc.) to be sure the product is safe to operate without danger of electrical shock.
   Do not use a line isolation transformer during this check.
   - Plug the AC line cord directly into the AC outlet. Using a "Leakage Current Tester", measure the leakage current from each exposed metal parts of the cabinet, particularly any exposed metal part having a return path to the chassis, to a known good earth ground. Any leakage current must not exceed 0.5mA AC (r.m.s.).
   - Alternate check method
     Plug the AC line cord directly into the AC outlet. Use an AC voltmeter having, 1,000 ohms per volt or more sensitivity in the following manner. Connect a 1,500Ω 10W resistor paralleled by a 0.15μF AC-type capacitor between an exposed metal part and a known good earth ground.
     Measure the AC voltage across the resistor with the AC voltmeter.
     Move the resistor connection to each exposed metal part, particularly any exposed metal part having a return path to the chassis, and measure the AC voltage across the resistor. Now, reverse the plug in the AC outlet and repeat each measurement. Voltage measured any must not exceed 0.75 V AC (r.m.s.). This corresponds to 0.5 mA AC (r.m.s.).




## Warning

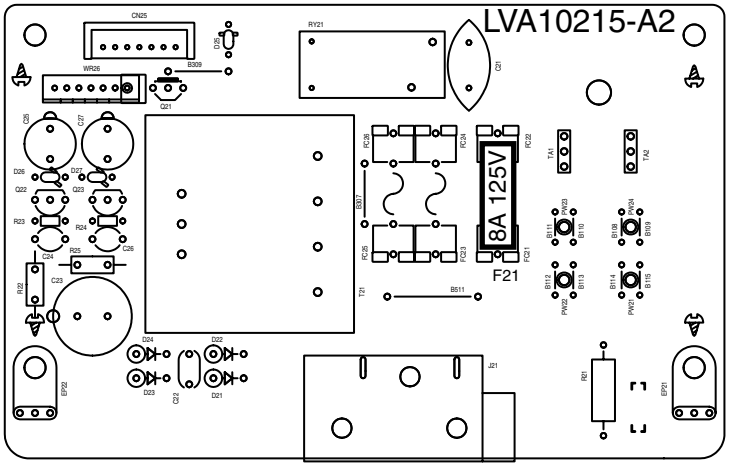
1. This equipment has been designed and manufactured to meet international safety standards.
2. It is the legal responsibility of the repairer to ensure that these safety standards are maintained.
3. Repairs must be made in accordance with the relevant safety standards.
4. It is essential that safety critical components are replaced by approved parts.
5. If mains voltage selector is provided, check setting for local voltage.

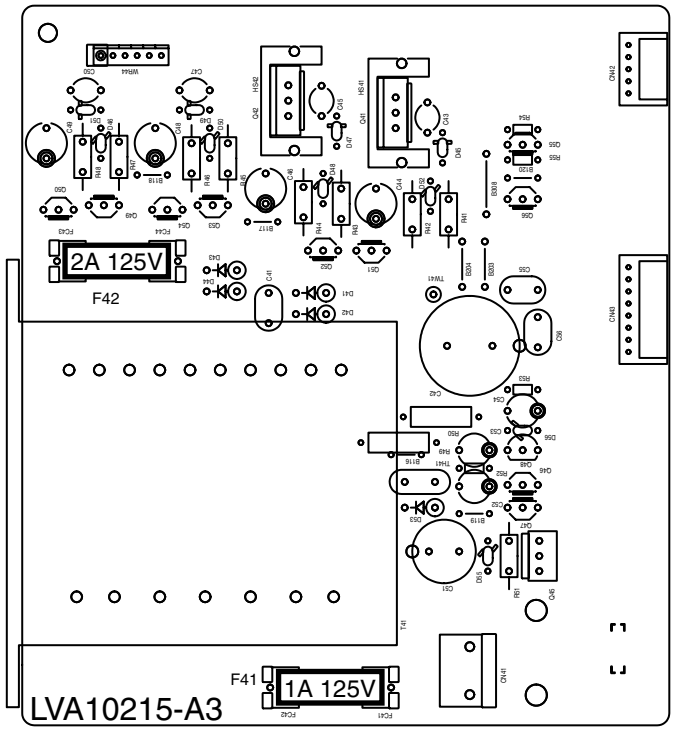
### ⚠ CAUTION

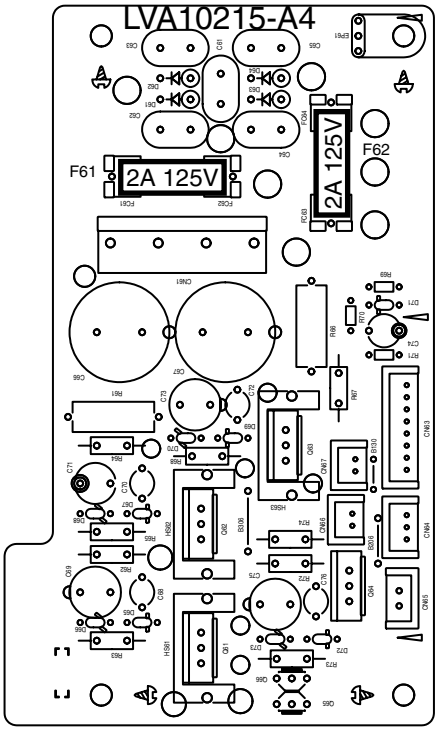
**Burrs formed during molding may be left over on some parts of the chassis. Therefore, pay attention to such burrs in the case of preforming repair of this system.**

In regard with component parts appearing on the silk-screen printed side (parts side) of the PWB diagrams, the parts that are printed over with black such as the resistor (▬), diode (▮) and ICP (●) or identified by the "⚠" mark nearby are critical for safety.
When replacing them, be sure to use the parts of the same type and rating as specified by the manufacturer. (Except the J&C version)

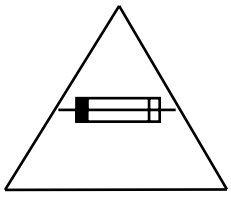
# Importance administering point on the safety




For USA and Canada / pour États - Unis d' Amérique et Canada



Caution: For continued protection against risk of fire, replace only with same type 1A/125V for F41, 2A/125V for F61, F62 and F42, 8A/ 125V for F21. This symbol specifies type of fast operating fuse.

Précaution: Pour eviter risques de feux, remplacez le fusible de sureté de et F41 comme le meme type que 1A/125V, et 2A/125V pour F61, F62 et F42, 8A/125V pour F21. Ce sont des fusibles sûretes qui functionnes rapide.

# Disassembly method

## ■ Removing the top cover (See Fig.1)

1. Remove the eight screws **A** attaching the top cover on both sides of the body.

2. Remove the three screws **B** on the back of the body.

3. Remove the top cover from behind in the direction of the arrow while pulling both sides outward.

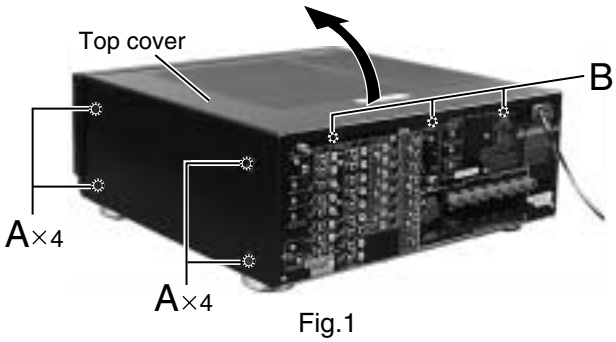


Fig.1

## ■ Removing the front panel assembly (See Fig.2 and 3)

- Prior to performing the following procedure, remove the top cover.

1. Cut off the tie band fixing the harness.

2. Disconnect the harness from the connector CN971, CN977, CN983 and CN985 on the front control board (see fig.5) and CN973 on the front AV in board (see Front panel assembly section/ fig.2).

3. Remove the screws **a** and **b**, and remove each earth wires.

4. Remove the three screws **C** attaching the front panel assembly.

5. Remove the four screws **D** attaching the front panel assembly on the bottom of the body. Detach the front panel assembly toward the front.

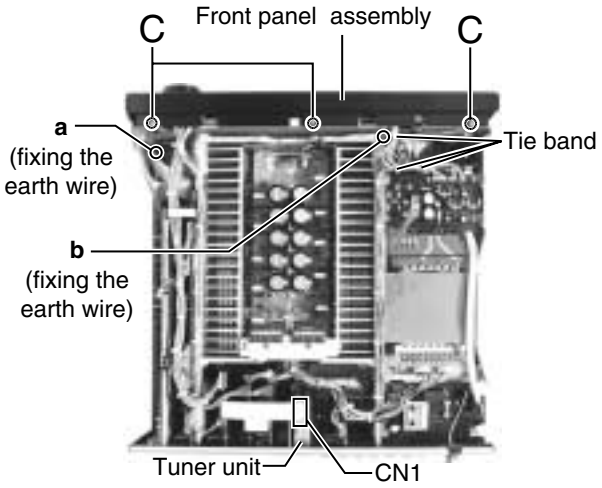


Fig.2

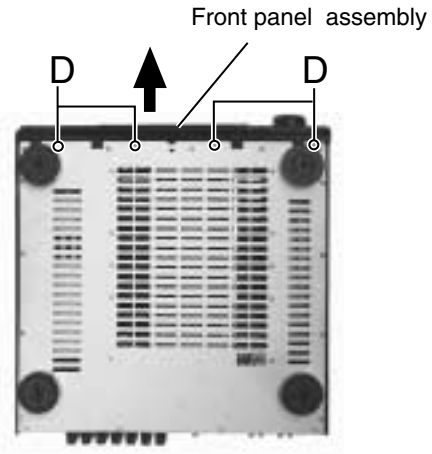


Fig.3

## ■ Removing the tuner unit (See Fig.2 and 4)

- Prior to performing the following procedure, remove the top cover.

1. Disconnect the card wire from the connector CN1 on the tuner unit.

2. Remove the two screws **E'** attaching the tuner unit to the rear panel.

## ■ Removing the rear panel (See Fig.4)

- Prior to performing the following procedure, remove the top cover.

1. Remove the power cord stopper from the rear panel by moving it in the direction of the arrow.

2. Remove the thirty screws **E** attaching the each boards to the rear panel on the back of the body.

3. Remove the thirteen screws **F** attaching the rear panel on the back of the body and bottom.

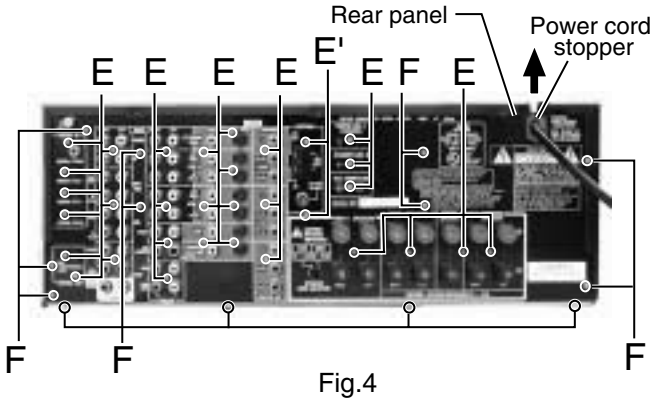


Fig.4

## ■ Removing the system control board (See Fig.5 and 6)

・ Prior to performing the following procedure, remove the top cover.

1. Disconnect the card wires and harness from connector CN963, CN964 and CN981 on the system control board.
2. Cut off the tie bands fixing the harnesses.
3. Disconnect the harness from connector CN43 on the power supply 2 board and CN25 on the power/ fuse board.
4. Disconnect the connector CN324 on the audio signal 2 board and CN205, CN234 on the audio signal 1 board.
5. Remove the three plastic rivet.

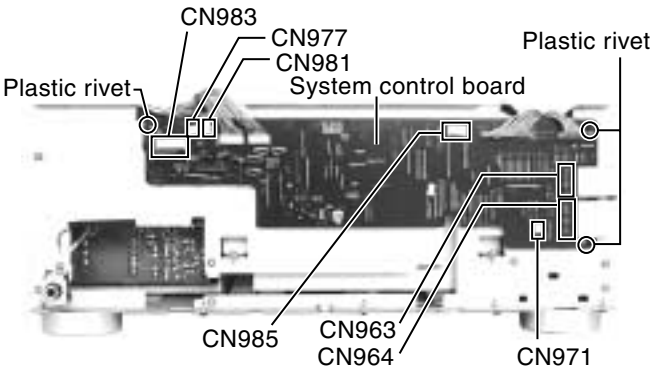



Fig.5

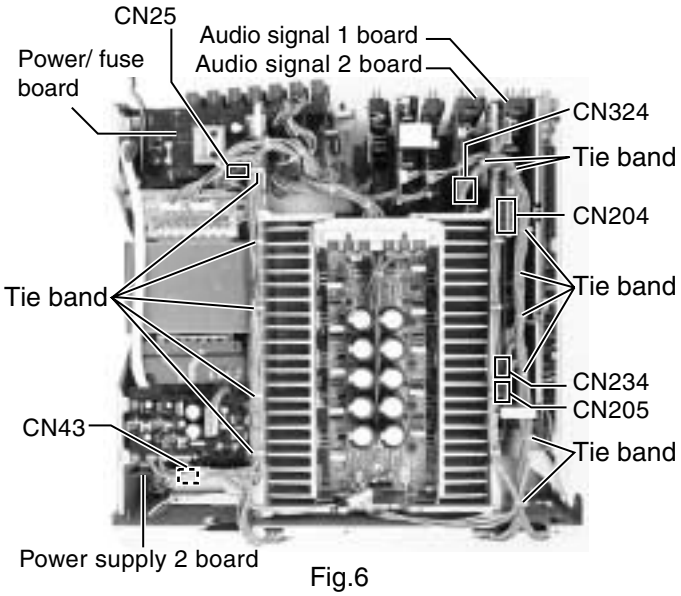



Fig.6

## ■ Removing the DSP board (See Fig.6 and 7)

・ Prior to performing the following procedure, remove the top cover and the rear panel.

1. Disconnect the connector CN631 on the DSP board.
2. Disconnect the connector CN204 on the audio signal 1 board.
3. Removing the two plastic rivet and disconnect the connector CN633 on the DSP board.

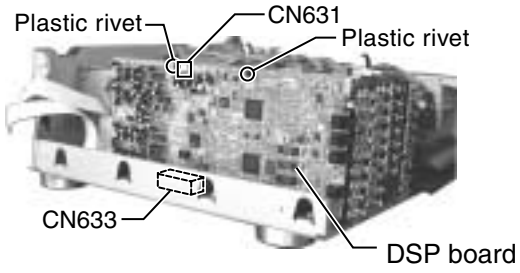



Fig.7

## ■ Removing the shield cover (See Fig.8)

・ Prior to performing the following procedure, remove the top cover and the rear panel.

1. Removing the screw **G** attaching the shield cover.
2. Shift the shield cover before, and pull upward.

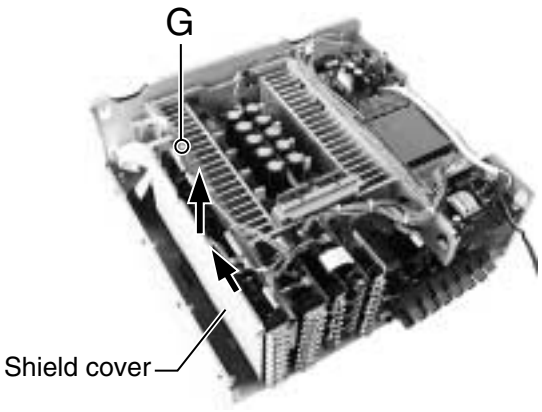



Fig.8

## ■Removing the audio signal 1 board (See Fig.9)

- Prior to performing the following procedure, remove the top cover, the rear panel and the DSP board.

1. Disconnect the harness from the connector CN224, CN207 and CN223 on the audio 1 board.
2. Removing the plastic rivet.
3. Disconnect the connector CN206 and CN221 on the audio 1 board.

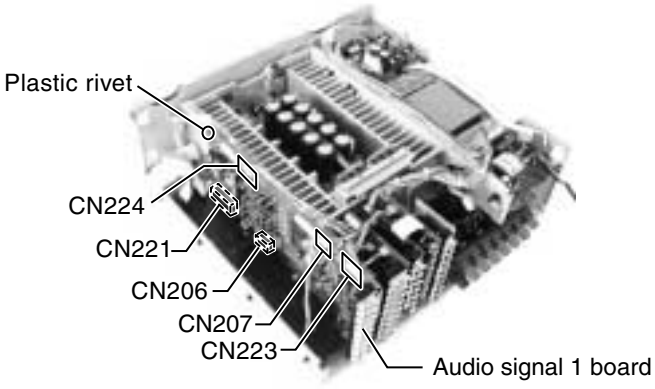



Fig.9

## ■Removing the audio signal 2 board & video board & s video board (See Fig.10 to 12)

- Prior to performing the following procedure, remove the top cover and the rear panel.

1. Disconnect the harness from connector CN973 on the front AV in board (see Front panel assembly section/ fig.2).
2. Cut off the tie band **c**.
3. Disconnect the harness from connector CN324 and CN323 on the audio signal 2 board.
4. Disconnect the connector CN321 and CN325. While removing the claw of the connector CN15, pull out the audio signal 2 board.

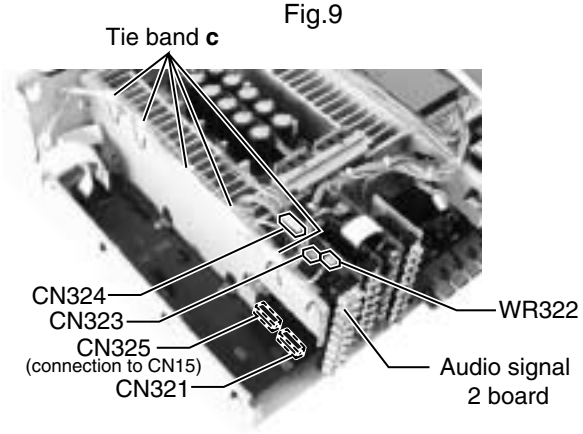



Fig.10

5. Cut off the tie band **d**.
6. Disconnect the card wire from connector CN402 on the video board.
7. Pull out the video board upward.

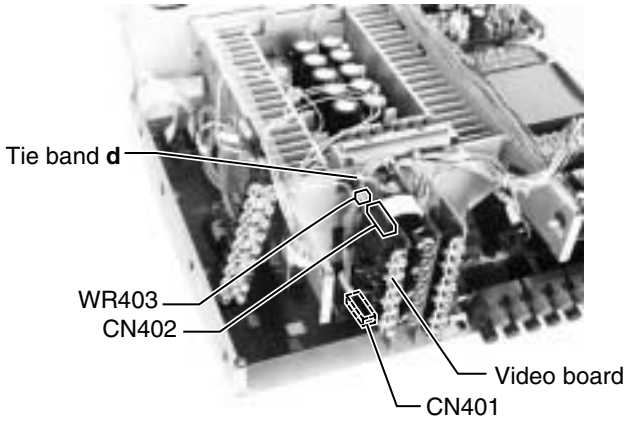



Fig.11

8. Cut off the tie band **e**.
9. Disconnect the card wire from connector CN432 on the s video board.
10. Disconnect the connector CN431 on the s video board. While removing the claw of the connector CN8, pull out the s video board.

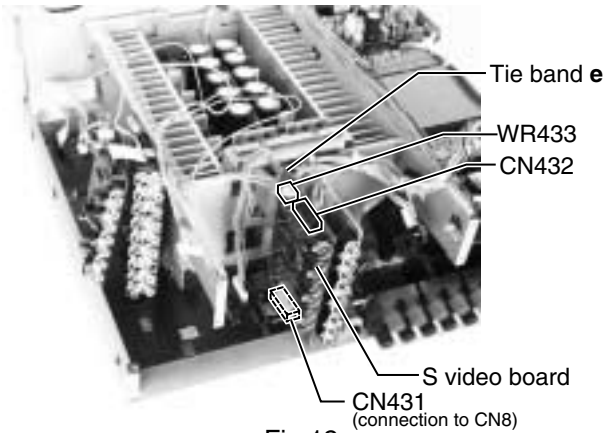



Fig.12

## ■ Removing the video SEP board (See Fig.13)

・ Prior to performing the following procedures, remove the top cover and the rear panel.

1. Disconnect the connector CN501 on the video SEP board. While removing the claw of the connector CN9, pull out the video SEP board.

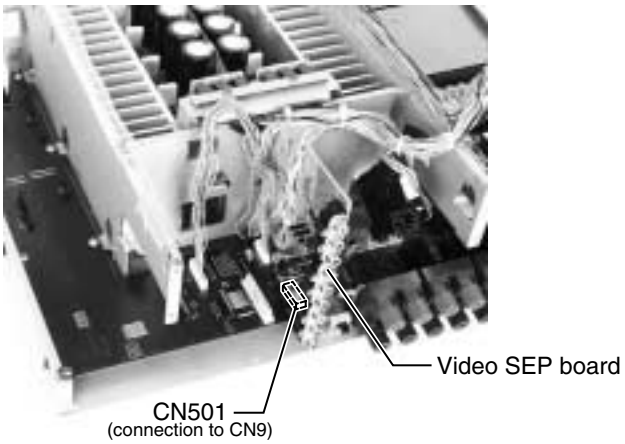



Fig.13

## ■ Removing the input base board (See Fig.14)

・ Prior to performing the following procedure, remove the top cover, rear panel, DSP board, audio signal 1 board, audio signal 2 board, video board and video SEP board.

1. Cut off the tie bands fixing the harnesses.
2. Disconnect the harnesses from the connector CN11 and CN16 on the input base board.
3. Disconnect the harnesses from the connector CN63 on the power supply 1 board and CN42 on the power supply 2 board.
4. Disconnect the harnesses from the connector CN 743 on the speaker board.
5. Remove the seven screws **H** attaching the input base board.

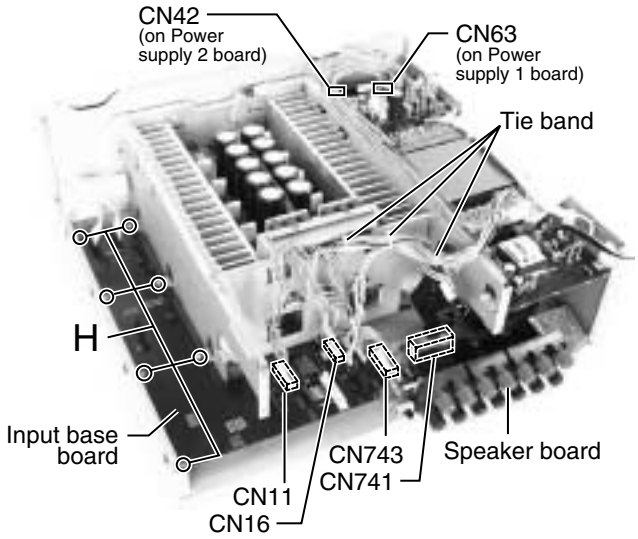



Fig.14

## ■ Removing the speaker board (See Fig.14)

・ Prior to performing the following procedure, remove the top cover and rear panel.

Attention : Speaker board is attached the rear panel by screws.

1. Cut off the tie band fixing the harnesses.
2. Disconnect the harnesses from the connector CN741 and CN743 on the speaker board.

## ■ Removing the compu link board (See Fig.15)

・ Prior to performing the following procedure, remove the top cover and rear panel.

Attention : Compu link board is attached the rear panel by screws.

1. Cut off the tie band fixing the harnesses.
2. Disconnect the harness from the connector CN301 on the compu link board.

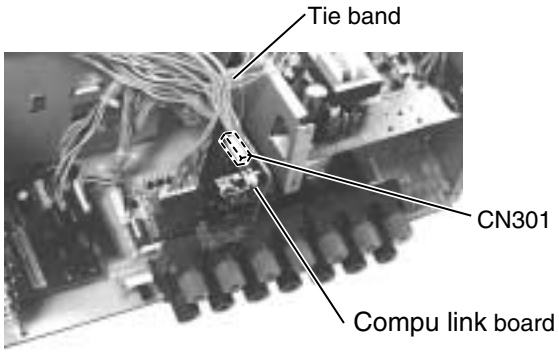



Fig.15

## ■Removing the power supply 1 board (See Fig.16)

- Prior to performing the following procedure, remove the top cover.

1. Disconnect the harnesses from the connector CN61, CN63, CN64 and CN65 on the power supply 1 board.

2. Remove the four screws **I** attaching the power supply 1 board.

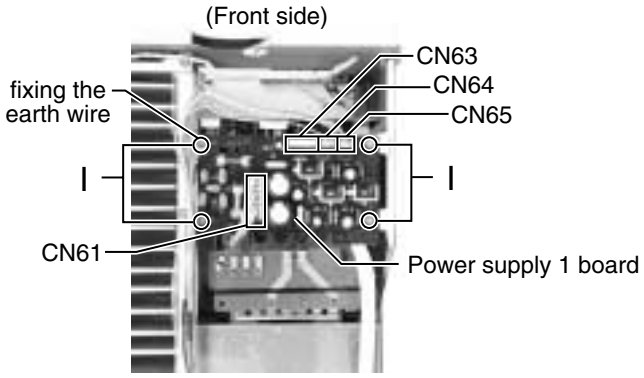



Fig.16

## ■Removing the regulator board (See Fig.17)

- Prior to performing the following procedure, remove the top cover and power supply 1 board.

1. Disconnect the harness from the connector CN45 on the regulator board.

2. Remove the screw **J** attaching the bracket and regulator board.

## ■ Removing the power transformer 1 (See Fig.17)

- Prior to performing the following procedure, remove the top cover and power supply 1 board.

1. Disconnect the harnesses from the connector CN41, CN42 and CN43 on the power supply 2 board and CN45 on the regulator board.

2. Remove the four screws **K** attaching the power transformer 1.

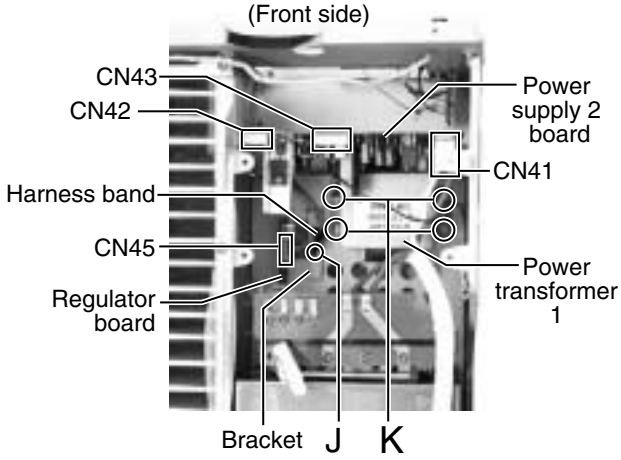



Fig.17

## ■Removing the power/ fuse board (See Fig.18)

- Prior to performing the following procedure, remove the top cover.

1. Unsolder the solder points TA1, TA2 and PW21, PW22, PW23, PW24 on the power/ fuse board.

2. Remove the four screws **L** attaching the power/ fuse board.

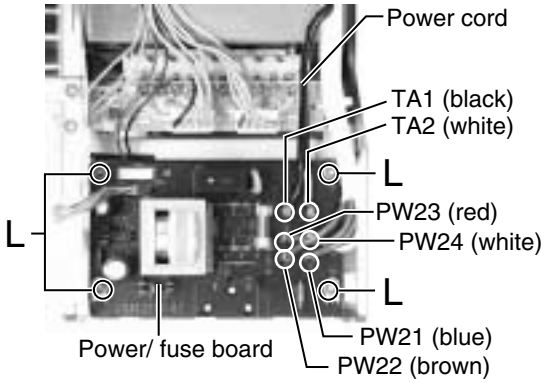



Fig.18

## ■Removing the power transformer 2 (See Fig.19)

- Prior to performing the following procedure, remove the top cover and power supply 1 board.

1. Disconnect the harnesses from the connector CN83 and CN84 on the power trans 2 board.

2. Unsolder the solder points PW81 and PW82 on the power supply 1 board.

3. Remove the four screws **M** attaching the power transformer 2.

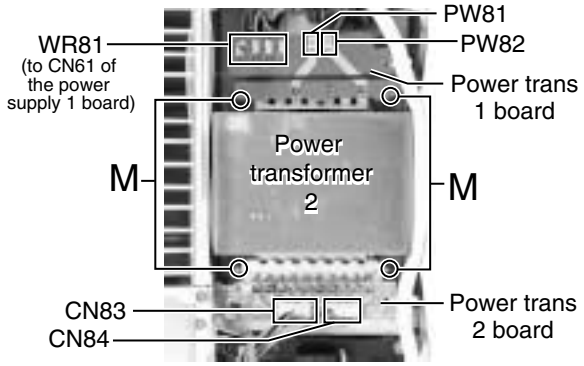



Fig.19

## ■ Removing the head phone board (See Fig.20 and 21)

・ Prior to performing the following procedures, remove the top cover, rear panel and front panel assembly.

1. Disconnect the harnesses from the connector CN981 on the system control board (see fig.5) and CN738 on the power amp. board.

2. Removing the nut **L** fixing the head phone board.

3. Removing the screw **M** attaching the earth wire and bracket.

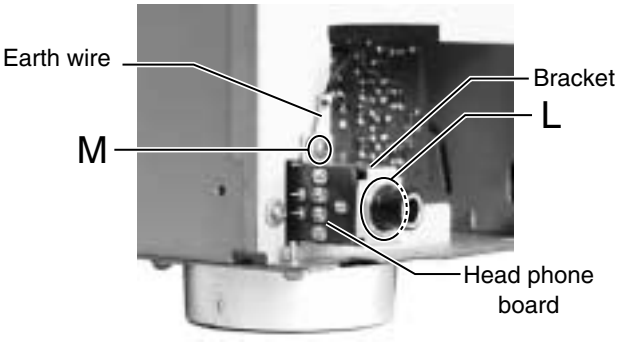



Fig.20

## ■ Removing the power amp. assembly (See Fig.21 and 22)

・ Prior to performing the following procedures, remove the top cover, rear panel, front panel assembly, system control board, DSP board, shield cover, audio signal 1 board, audio signal 2 board, video board, s video board and input base board.

1. Remove the three screws **N** fixing the barriers, and remove the tow barriers.

2. Remove the eight screws **O** attaching the power amp. assembly.

3. Pull up the power amp. assembly.

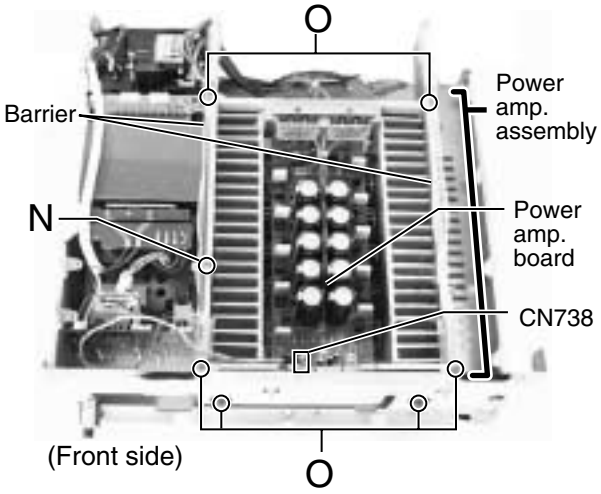



Fig.21

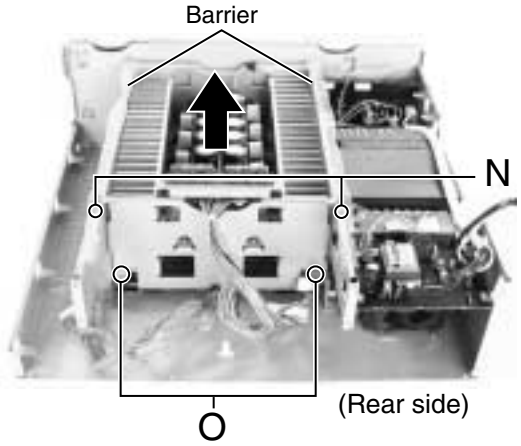



Fig.22

## ■ Removing the fan motor (See Fig.23)

・ Prior to performing the following procedures, remove the top cover and rear panel.

1. Disconnect the harness from the connector CN65 on the power supply 1 board (see fig.16).

2. Removing the four screws **P** attaching the fan motor.

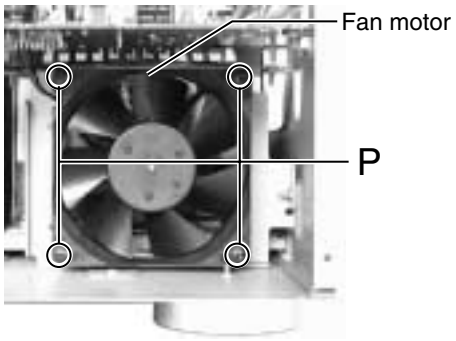



Fig.23

## <Power amp. assembly section>

### ■Removing the relay board (See Fig.1)

- Prior to performing the following procedure, remove the power amp. assembly.

1. Place the bottom side upward.
2. Remove the harness band and cut off the tie bands.
3. Remove the two screws **A** attaching the relay board.
4. Disconnect the connector CN721, CN821, CN781 and CN761.

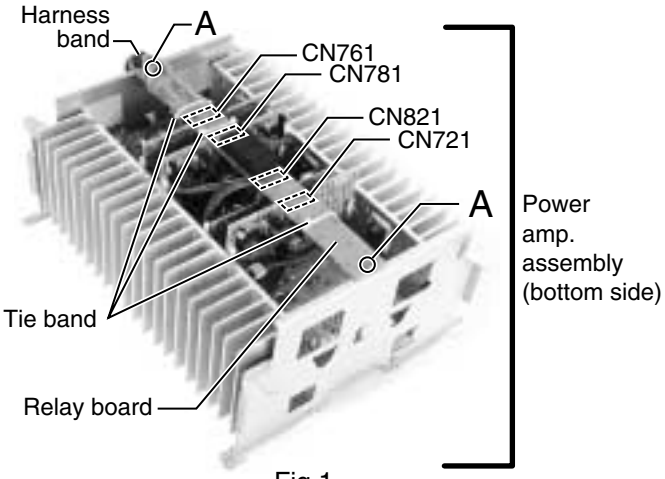



Fig.1

### ■Removing the Rch pre amp. & Lch pre amp. & center pre amp. & surround pre amp. (See Fig.2)

- Prior to performing the following procedure, remove the power amp. assembly and relay board.

1. Disconnect the harness from five connectors CN70 on the thermal compensation board.
2. Pull out each pre amp. board upward.

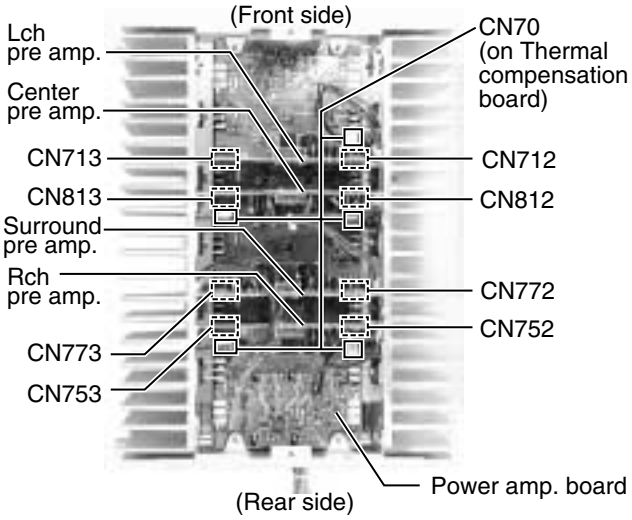



Fig.2

### ■Removing the heat sink (See Fig.3 and 4)

- Prior to performing the following procedure, remove the power amp. assembly, relay board and each pre amp. board.

1. Remove the eight screws **B** attaching the heat sink both side.
2. Remove the ten screws **C** attaching the power ICs.

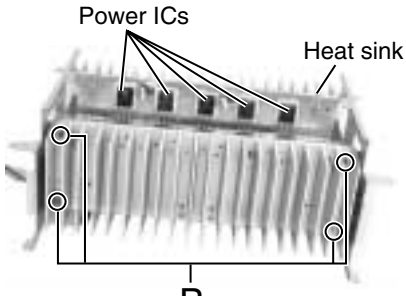



Fig.3

### ■Removing the amp. sub Lo & amp. sub Hi board (See Fig.5)

- Prior to performing the following procedure, remove the power amp. assembly.

1. Remove the two screws **D** attaching the bracket.

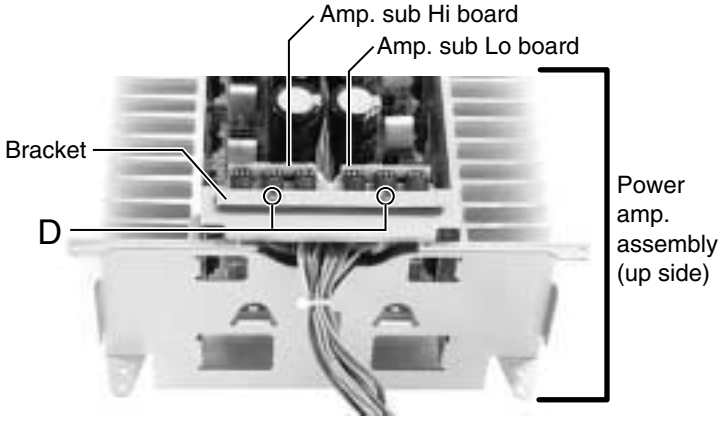



Fig.5

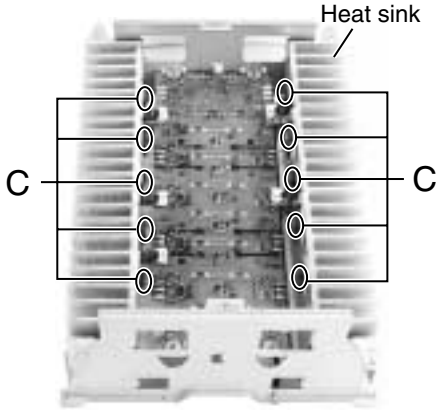



Fig.4

## <Front panel assembly section>

### ■Removing the FL display board & front AV in board (See Fig.1 and 2)

- Prior to performing the following procedure, remove the top cover and the front panel assembly.

1. Pull out the volume knob on the front side of the front panel assembly and remove the nut attaching the FL display board.
2. Disconnect the harness from the connector CN973 on the front AV in board.
3. Remove the three screws **A** attaching the front AV in board.
4. Disconnect the harnesses from connector CN969, CN975 and CN982 on the FL display board.
5. Remove the nine screws **B** attaching the FL display board on the back of the front panel.

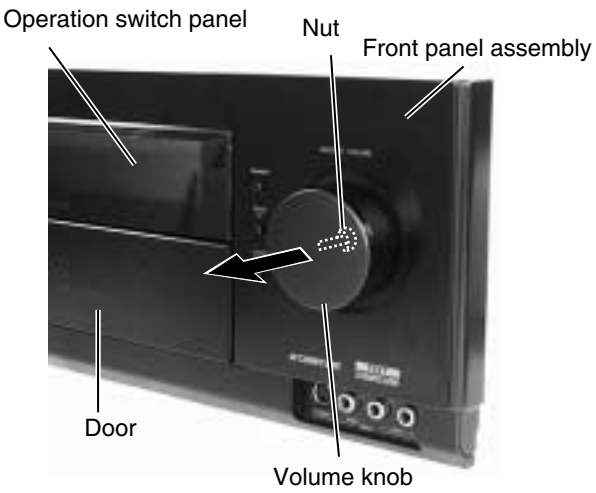


Fig.1

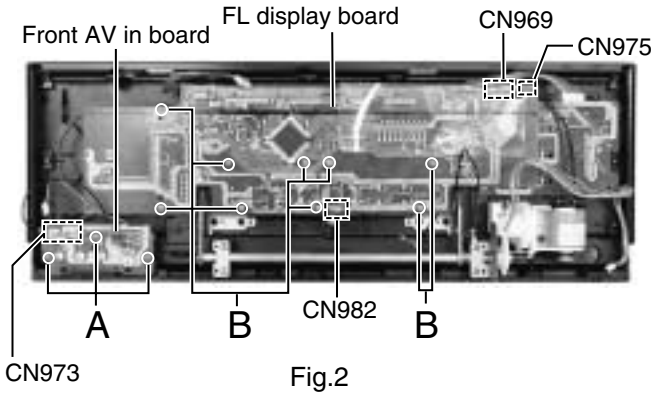


Fig.2

### ■Removing the power switch board & motor assembly (See Fig.3)

- Prior to performing the following procedure, remove the front panel assembly and the FL display board.

1. Remove the four screws **C** attaching the power switch board.
2. Remove the three screws **D** attaching the motor assembly on the back of the front panel.
3. Remove the belt and the two screws **a** attaching the motor.

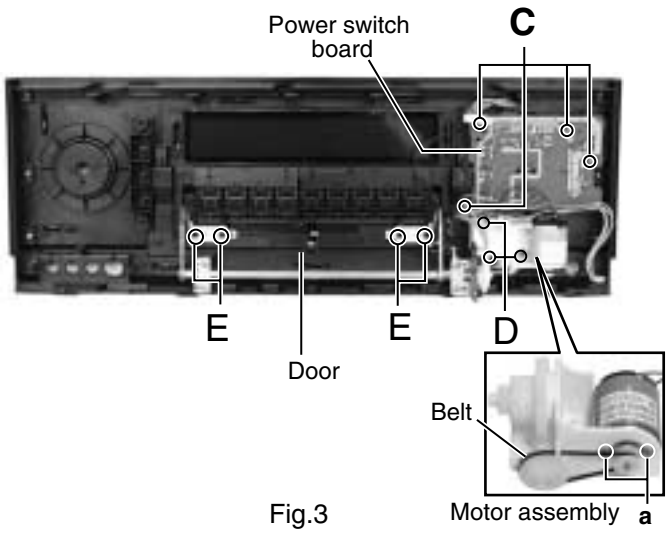


Fig.3

### ■Removing the door input board (See Fig.3 and 4)

- Prior to performing the following procedure, remove the front panel assembly and the FL display board.

1. Remove the four screws **E** attaching the door and remove the door from front panel assembly.
2. Remove the six screws **F** attaching the door input board.

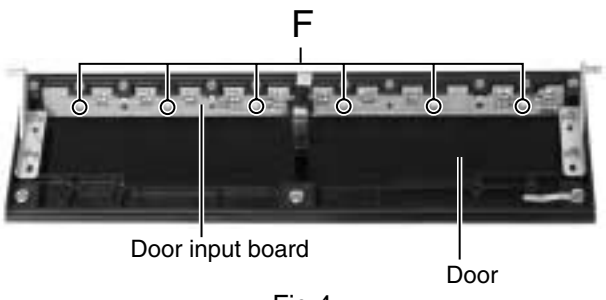


Fig.4

# Adjustment method

## ■ Power amplifier section

**Adjustment of idling current**

| /// Measuring point /// | | /// Alignment point /// | | *** Measurig condition *** |
|---|---|---|---|---|
| Lch | : B903 & B904 | Lch | : VR701 | • No load, No signal and Rated line voltage |
| Rch | : B911 & B912 | Rch | : VR751 | • SURROUND : OFF |
| Cch | : B907 & B908 | Cch | : VR801 | • Speaker load SW : HIGH |
| SLch | : B905 & B906 | SLch | : VR771 | |
| SRch | : B909 & B910 | SRch | : VR772 | • Room temperature : 20~25℃ |

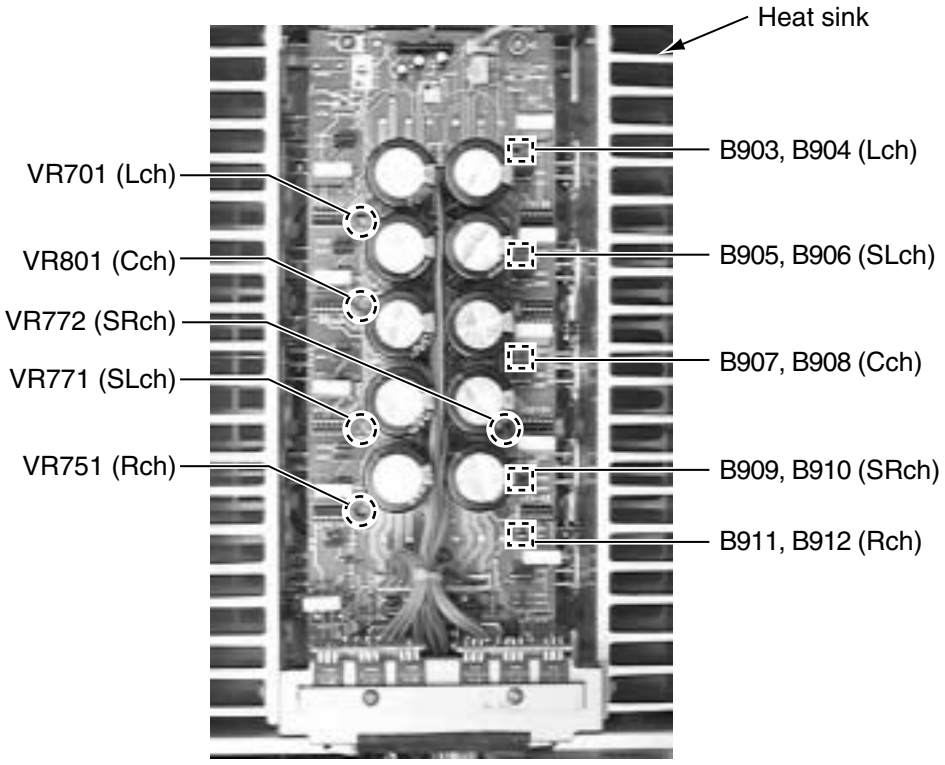
**Attention**
**This adjustment does not obtain a correct adjustment value immediately after the amplifier is used (state that an internal temperature has risen).**
**Please adjust immediately after using the amplifier after turning off the power supply of the amplifier and falling an internal temperature.**

<Adjustment method>

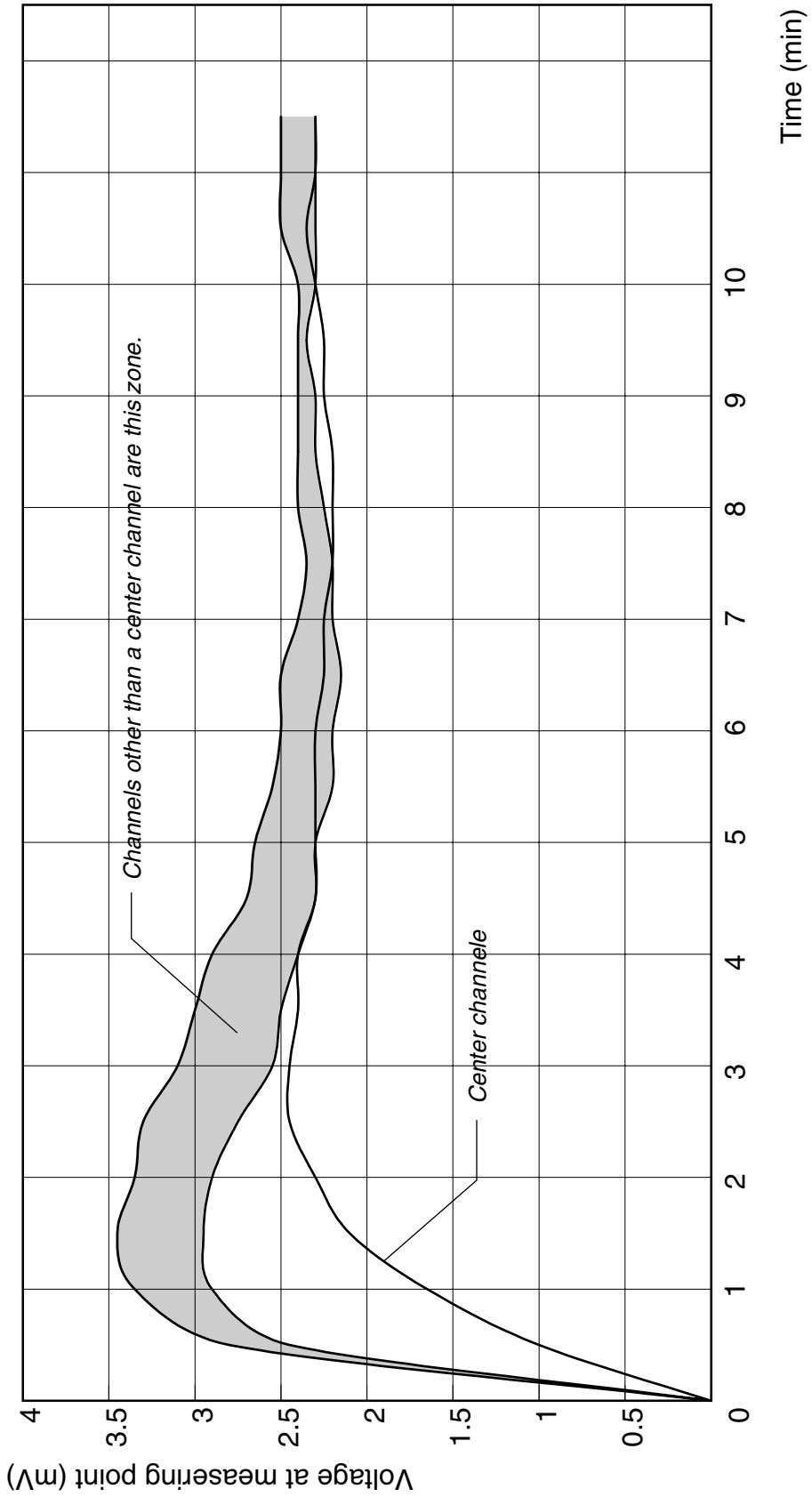
1. Prior to turning the power ON, fully turn the adjusting resistor (VR701,VR751,VR771,VR772,VR801) counterclockwise direction and connect the DC voltmeter to the measuring terminal (B903-B904, B905-B906, B907-B908, B909-B910, B911-B912).
2. Adjust the resistor so that the measured value becomes 2.0mV just after the power supply is turned on.
3. Adjust the resistor so that the measured value becomes 2.5mV more than 60 seconds after the power supply is turned on.
4. After stability is 1.0-4.0mV.

The "idling current" graph of the following page is referred to.

* It is not abnormal though the idling current might not become 0mA even if it is finished to turn variable resistance (VR701,VR751,VR771,VR772,VR801) in the direction of counterclockwise.



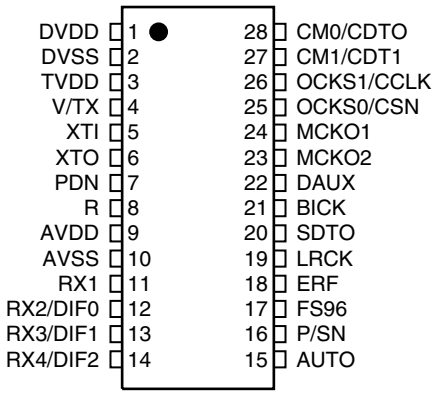
**RX-DP9 Idling Current**



# Description of major ICs

## ■ AK4112 (IC673) : Digital audio receiver

1.Pin layout

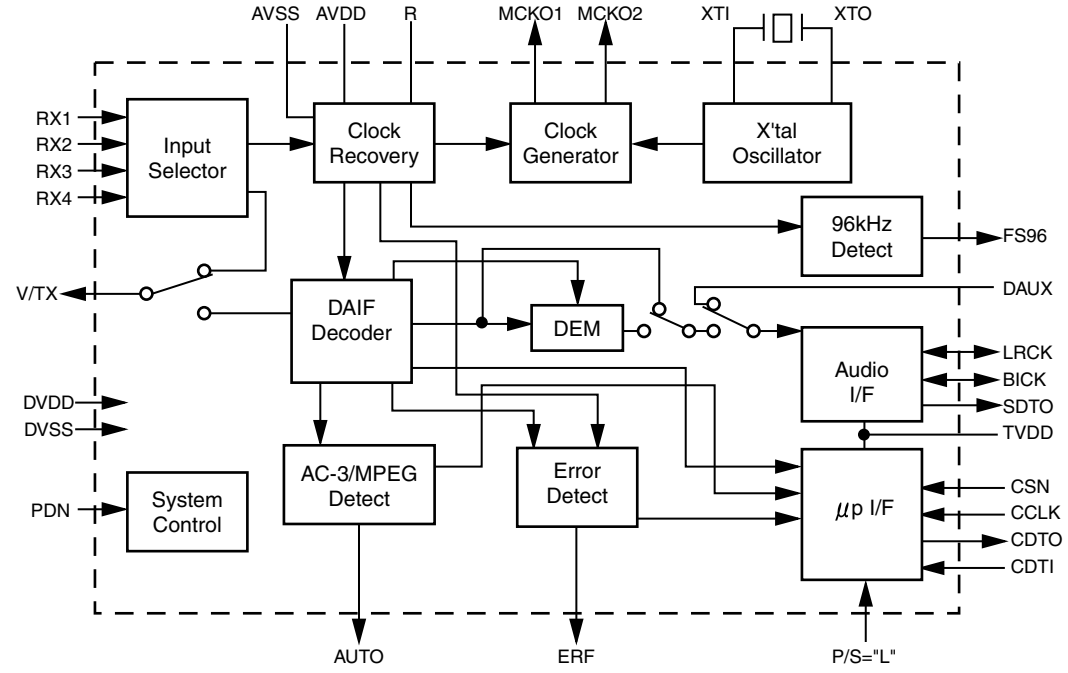



2.Pin function

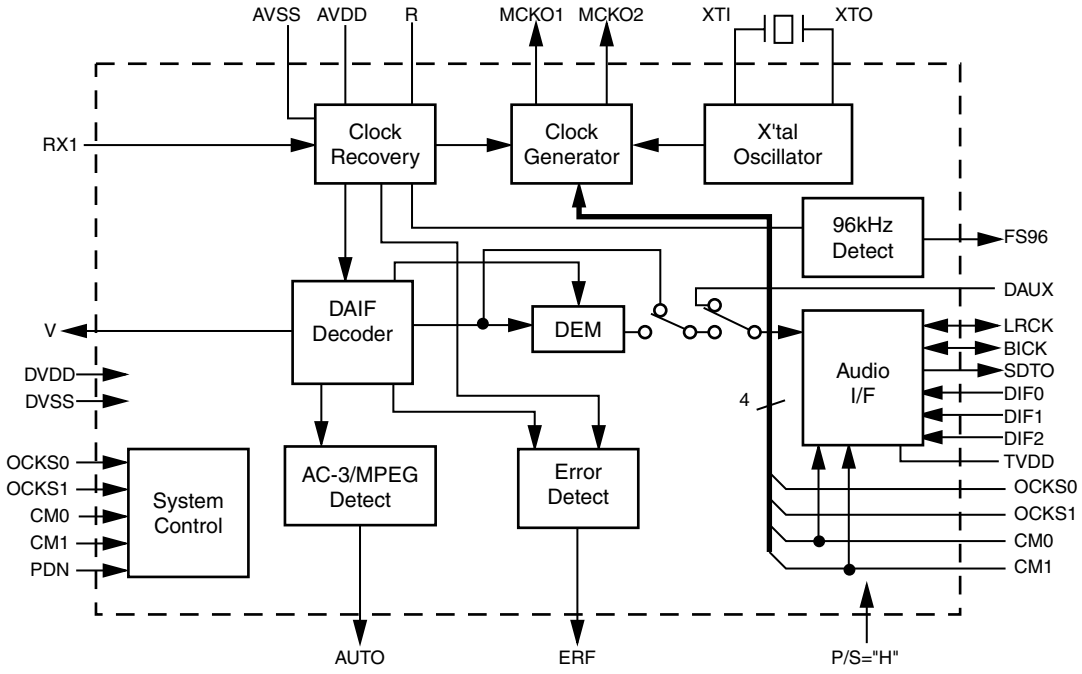
| Pin No. | Symbol | I/O | Function |
|---|---|---|---|
| 1 | DVDD | - | Digital Power Supply Pin, 3.3V |
| 2 | DVSS | - | Digital Ground Pin |
| 3 | TVDD | - | Input Buffer Power Supply Pin, 3.3V or 5V |
| 4 | V | O | Validity Flag Output Pin in Parallel Mode |
| | TX | O | Transmit channel (through data) Output Pin in Serial Mode |
| 5 | XTI | I | X'tal Input Pin |
| 6 | XTO | O | X'tal Output Pin |
| 7 | PDN | I | Power-Down Mode PIn |
| | | | When "L", the AK4112A is powered-down and reset. |
| 8 | R | - | External Resistor Pin |
| | | | 18kΩ +/-1% resistor to AVSS externally. |
| 9 | AVDD | - | Analog Power Supply Pin |
| 10 | AVSS | - | Analog Ground Pin |
| 11 | RX1 | I | Receiver Channel 1 |
| | | | This channel is selected in Parallel Mode or default of Serial Mode. |
| 12 | RX2 | I | Audio Data Interface Format 0Pin in Parallel Mode |
| | DIF0 | I | Receiver Channel 2 in Serial Mode |
| 13 | RX3 | I | Audio Data Interface Format 1 Pin in Parallel Mode |
| | DIF1 | I | Receiver Channel 3 in Serial Mode |
| 14 | RX4 | I | Audio Data Interface Format 2 Pin in Parallel Mode |
| | DIF2 | I | Receiver Channel 4 in Serial Mode |
| 15 | AUTO | O | Non-PCM Detect Pin |
| | | | "L": No detect, "H": Detect |
| 16 | P/S | I | Parallel/Serial Select Pin |
| | | | "L": Serial Mode, "H": Parallel Mode |
| 17 | FS96 | O | 96kHz Sampling Detect Pin |
| | | | (RX Mode) "H": fs=88.2kHz or more, "L": fs=54kHz or less. |
| | | | (X'tal Mode) "H": XFS96=1, "L": XFS96=0. |
| 18 | ERF | O | Unlock & Parity Error Output Pin |
| | | | "L": No Error, "H": Error |
| 19 | LRCK | I/O | Output Channel Clock Pin |
| 20 | SDTO | O | Audio Serial Data Output Pin |
| 21 | BICK | I/O | Audio Serial Data Clock Pin |
| 22 | DAUX | I | Auxiliary Audio Data Input Pin |
| 23 | MCK02 | O | Master Clock #2 Output Pin |
| 24 | MCK01 | O | Master Clock #1 Output Pin |
| 25 | OCKS0 | I | Output Clock Select 0 Pin in Parallel Mode |
| | CSN | I | Chip Select Pin in Serial Mode |
| 26 | OCKS1 | I | Output Clock Select 1 Pin in Parallel Mode |
| | CCLK | I | Control Data Clock Pin in Serial Mode |
| 27 | CM1 | I | Master Clock Operation Mode Pin0 in Parallel Mode |
| | CDTI | I | Control Data Input Pin in Serial Mode |
| 28 | CM0 | I | Master Clock Operation Mode Pin1 in Parallel Mode |
| | CDTO | O | Control Data Output Pin in Serial Mode |

Note 1: All input pins except internal pull-down pins should not be left floating.

3.Block diagram



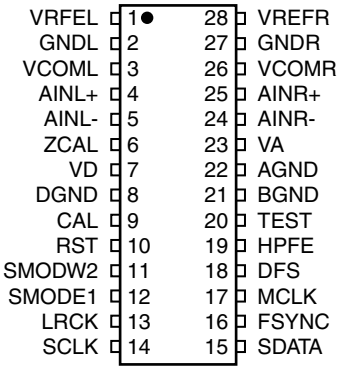

Serial Control Mode



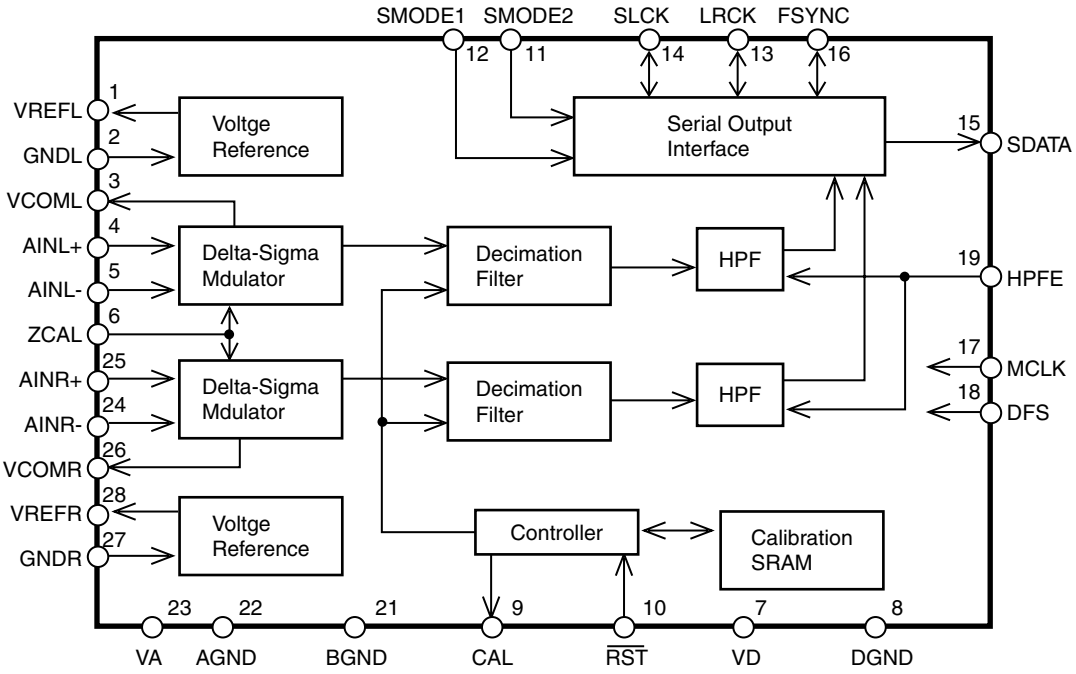

Parallel Control Mode

## ■AK5383VF (IC657) : A/D converter

1. Pin layout




2. Block diagram




3. Pin function (1/2)

| Pin No. | Pin name | I/O | Function |
|---|---|---|---|
| 1 | VRFEL | O | Lch Reference Voltage Pin, 3.75V<br>Normally connected to GNDL with a 10μF electrolytic capacitor and a 0.1μF ceramic capacitor. |
| 2 | GNDL | - | Lch Reference Ground Pin, 0V |
| 3 | VCOML | O | Lch Common Voltage Pin, 2.75V |
| 4 | AINL+ | I | Lch Analog positive input Pin |
| 5 | AINL- | I | Lch Analog negative input Pin |
| 6 | ZCAL | I | Zero Calibration Control Pin<br>This pin controls the calibration reference signal.<br>"L": VCOML and VCOMR<br>"H": Analog Input Pins (AINL±, AINR±) |
| 7 | VD | - | Digital Power Supply Pin, 3.3V |
| 8 | DGND | - | Digital Ground Pin, 0V |

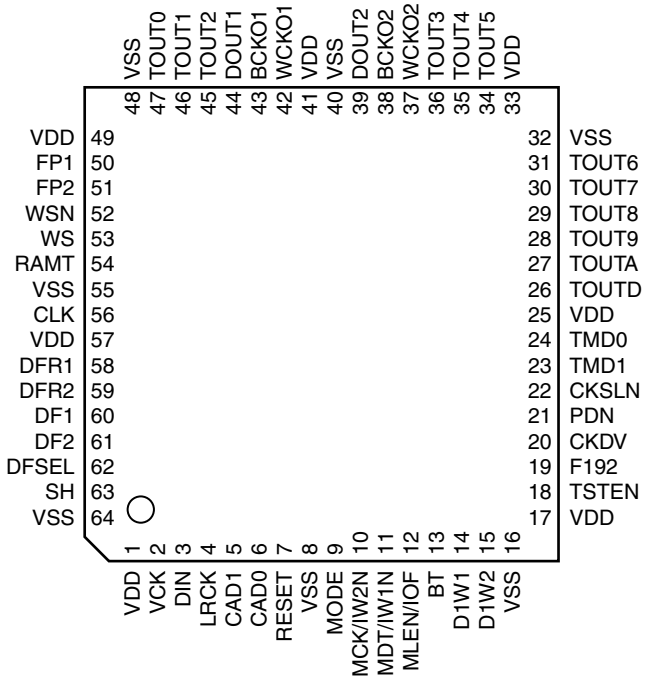
3. Pin function (2/2)

| Pin No. | Pin name | I/O | Function |
|---|---|---|---|
| 9 | CAL | O | Calibration Active Signal Pin<br>"H" means the offset calibration cycle is in progress. Offset calibration starts when RST goes "H". CAL goes "L" after 8704 LRCK cycles for DFS="L", 17408 LRCK cycles for DFS="H". |
| 10 | RST | I | Reset Pin<br>When "L", Digital section is powered-down. Upon returning "H", an offset calibration cycle is started. An offset calibration cycle should always be initiated after power-up. |
| 11<br>12 | SMODW2<br>SMODE1 | I<br>I | Serial Interface Mode Select Pin<br>MSB first, 2's compliment.<br>SMODE2 SMODE1 MODE LRCK<br>L L Slave mode : MSB justified : H/L<br>L H Master mode : Similar to I2S : H/L<br>H L Slave mode :I2S : L/H<br>H H Master mode : I2S : L/H |
| 13 | LRCK | I/O | Left/Right Channel Select Clock Pin<br>LRCK goes "H" at SMODE2="L" and "L" at SMODE2="H" during reset when SMODE1 "H". |
| 14 | SCLK | I/O | Serial Data Clock Pin<br>Data is clocked out on the falling edge of SCLK.<br>Slave mode:<br>SCLK requires more than 48fs clock.<br>Master mode:<br>SCLK outputs a 128fs(DFS="L") or 64fs (DFS="H")clock.<br>SCLK stays "L" during reset. |
| 15 | SDATA | O | Serial Data Output Pin<br>MSB first, 2's complement. SDATA stays "L" during reset. |
| 16 | FSYNC | I/O | Frame Synchronization Signal Pin<br>Slave mode:<br>When "H", the data bits are clocked out on SDATA. In I2S mode, FSYNC is Don't care.<br>Master mode:<br>FSYNC outputs 2fs clock. FSYNC stays "L" during reset. |
| 17 | MCLK | I | Master Clock Input Pin<br>256fs at DFS="L", 128fs at DFS="H". |
| 18 | DFS | I | Double Speed Sampling mode Pin<br>"L": Normal Speed "H": Double Speed |
| 19 | HPFE | I | High Pass Filter Enable Pin<br>"L": Disable "H": Enable |
| 20 | TEST | I | Test Pin (pull-down pin)<br>Should be connected to GND. |
| 21 | BGND | - | Substrate Ground Pin, 0V |
| 22 | AGND | - | Analog Ground Pin, 0V |
| 23 | VA | - | Analog Supply Pin, 5V |
| 24 | AINR- | I | Rch Analog negative input Pin |
| 25 | AINR+ | I | Rch Analog positive input Pin |
| 26 | VCOMR | O | Rch Common Voltage Pin, 2.75V |
| 27 | GNDR | - | Rch Reference Ground Pin, 0V |
| 28 | VREFR | O | Rch Reference Voltage Pin, 3.75V<br>Normally connected to GNDR with a 10μF electrolytic capacitor and a 0.1 F ceramic capacitor |

Note: All digital inputs should not be left floating.

## ■ JVC8006 (IC635) : CC converter

1. Pin layout




3. Pin function (1/2)

| Pin No. | Pin name | I/O | Function |
|---|---|---|---|
| 1 | VDD | - | Power supply : All VDD pins must be connected externally |
| 2 | BCK | I1 | Bit clock input :Bit click if serial data into the DIN ; Must run continuously, "5V tolerant" |
| 3 | DIN | I1 | Serial audio data input, "5V tolerant" |
| 4 | LRCK | I1 | Left/Right clock input ; sampling frequency (fs) for DIN ; Must run continuously, "5V tolerant" |
| 5 | CAD1 | Ip2 | Chip address 1 ; available on MODE=H |
| 6 | CAD0 | Ip2 | Chip address 0 ; available on MODE=H |
| 7 | RESET | I1 | System reset ; the internal state is reset to the default setting when L, "5V tolerant" |
| 8 | VSS | - | Ground ; All VSS pins must be connected externally |
| 9 | MODE | Ip2 | System control mode select input : (H=Software mode ; L=Hardware mode) |
| 10 | MCK/IW2N | I1 | Control clock input ; MODE=H, |
| | | | /Select input audio data word length input2 ; MODE=L, "5V tolerant" |
| 11 | MDT/IW1N | I1 | Control data input ; MODE=H, |
| | | | /Select input audio data word length input 1 ; MODE=L, "5V tolerant" |
| 12 | MLEN/IOF | I1 | Control data latch input ; MODE=H, |
| | | | /select input and output audio data format input ; MODE=L, "5V tolerant" |
| 13 | BTR | Ip2 | Select BIT-UP through mode input ; MODE=L |
| 14 | D1W1 | Ip2 | Select output 1 audio data word length and enable control 1 ; MODE=L |
| 15 | D1W2 | Ip2 | Select output 1 audio data word length and enable control 2 ; MODE=L |
| 16 | VSS | - | Ground ; All VSS pins must be connected externally |
| 17 | VDD | - | Power supply ; All VSS pins must be connected externally |
| 18 | TSTEN | Ip2 | Test control input ; in normal operation this pin should be terminated to ground |
| 19 | F192 | Ip2 | Select system clock for 192kHz input sampling frequency input : MODE=L, |
| | | | (supported for FS-UP only) |
| 20 | CKDV | Ip2 | Internal click divider select input ; MODE=L,(L=1, H=1/2) |

I=CMOS, I1=Schmitt, Ip2=Schmitt with pull-down resistor, O=CMOS (H=VDD, L=VSS)

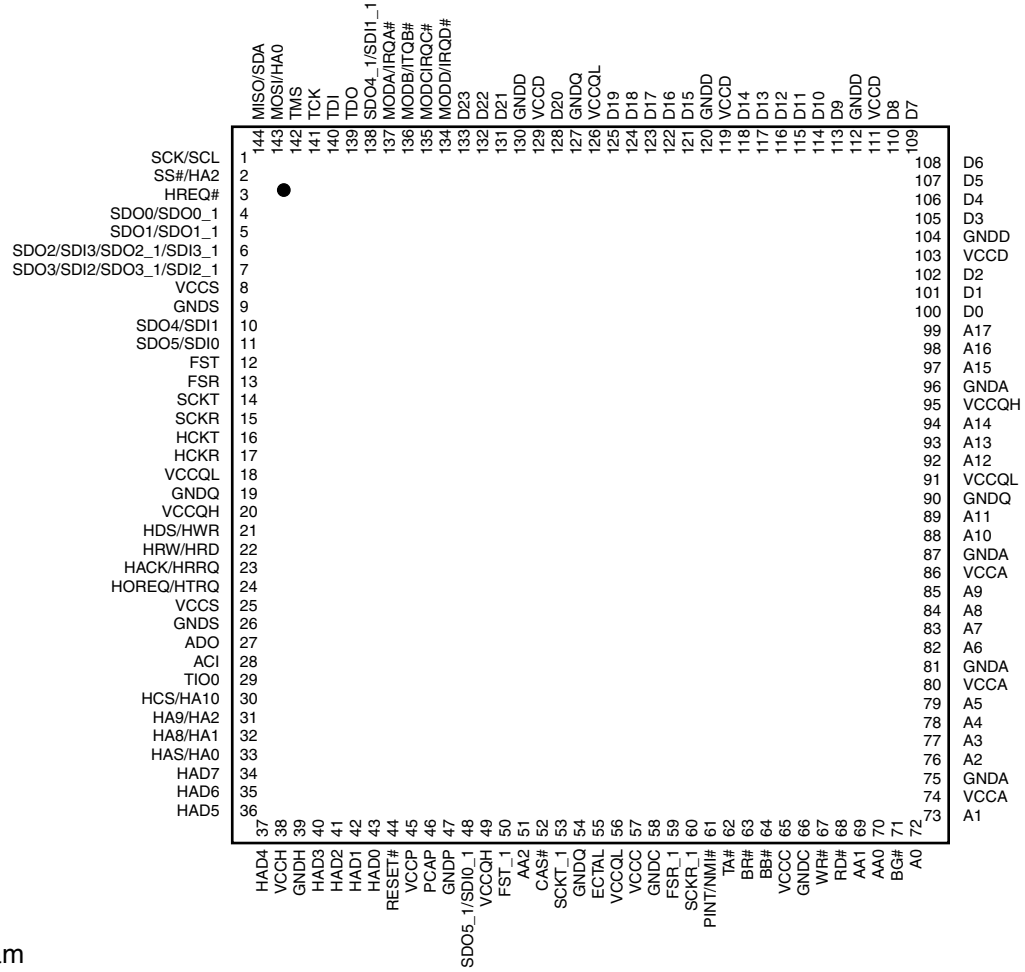
2. Pin function (2/2)

| Pin No. | Pin name | I/O | Function |
|---|---|---|---|
| 21 | PDN | Ip2 | Power down control input ; MODE=L, (L=normal, H=power down) |
| 22 | CKSLN | Ip2 | System clock select input ; MODE=L, (L=512fs, H=384fs) |
| 23 | TMD1 | Ip2 | Test input ; in normal operation this pin should be terminated to ground |
| 24 | TMD0 | Ip2 | Test input ; in normal operation this pin should be terminated to ground |
| 25 | VDD | - | Power supply ; All VDD pins must be connected externally |
| 26 | TOUTD | O | Test output ; this pin should be left open |
| 27 | TOUTA | O | Test output ; this pin should be left open |
| 28 | TOUT9 | O | Test output ; this pin should be left open |
| 29 | TOUT8 | O | Test output ; this pin should be left open |
| 30 | TOUT7 | O | Test output ; this pin should be left open |
| 31 | TOUT6 | O | Test output ; this pin should be left open |
| 32 | VSS | - | Ground ; All VSS pins must be connected externally |
| 33 | VDD | - | Power supply ; All VDD pins must be connected externally |
| 34 | TOUT5 | O | Test output ; this pin should be left open |
| 35 | TOUT4 | O | Test output ; this pin should be left open |
| 36 | TOUT3 | O | Test output ; this pin should be left open |
| 37 | WCKO2 | O | L/R clock output 2 ; the left or right channel for the DOUT2 |
| 38 | BCKO2 | O | Bit clock output 2 ; bit clock of serial data for the DOUT2 |
| 39 | DOUT2 | O | Serial audio data output 2 |
| 40 | VSS | - | Ground ; All VSS pins must be connected externally |
| 41 | VDD | - | Power supply ; All VDD pins must be connected externally |
| 42 | WCKO1 | O | L/R clock output 1 ; the left or right channel for the DOU 1 |
| 43 | BCKO1 | O | Bit clock output 1; bit clock of serial data for the DOUT1 |
| 44 | DOUT1 | O | Serial audio output 1 |
| 45 | TOUT2 | O | Test output ; this pin should be left open |
| 46 | TOUT1 | O | Test output ; this pin should be left open |
| 47 | TOUT0 | O | Test output ; this pin should be left open |
| 48 | VSS | - | Ground ; All VSS pins must be connected externally |
| 49 | VDD | - | Power supply ; All VDD pins must be connected externally |
| 50 | FP1 | Ip2 | Select FS-UP peak data compensation coefficient input 1 ; MODE=L |
| 51 | FP2 | Ip2 | Select FS-UP peak data compensation coefficient input 2 ; MODE=L |
| 52 | WSN | Ip2 | Select FS-UP waveform compensation function control for 16fd to 9fd input ; MODE=L |
| 53 | WS | Ip2 | Select FS-UP waveform compensation function control for 8fd to 2fd input ; MODE=L |
| 54 | RAMT | Ip2 | RAM test control input ; in normal operation this pin should be terminated to ground |
| 55 | VSS | - | Ground ; All VSS pins must be connected externally |
| 56 | CLK | I | Master clock input ; Must run continuously normal operation, "5V tolerant" |
| 57 | VDD | - | Power supply ; All VDD pins must be connected externally |
| 58 | DFR1 | Ip2 | Select DF over sampling rate control 1 input for FS-UP and output 2 ; MODE=L |
| 59 | DFR2 | Ip2 | Select DF over sampling rate control 2 input for FS-UP and output 2 ; MODE=L |
| 60 | DF1 | Ip2 | Select DF over sampling rate control 1 input for output 1 ; MODE=L |
| 61 | DF2 | Ip2 | Select DF over sampling rate control 2 input for output 1 ; MODE=L |
| 62 | DFSEL | Ip2 | Select DF internal digital fitter ; MODE=L, (L=84tap FIR, H=169tap FIR) |
| 63 | SH | Ip2 | Select SH mode control input ; MODE=L, (L=ON, H=OFF) |
| 64 | VSS | - | Ground ; All VSS pins must be connected externally |

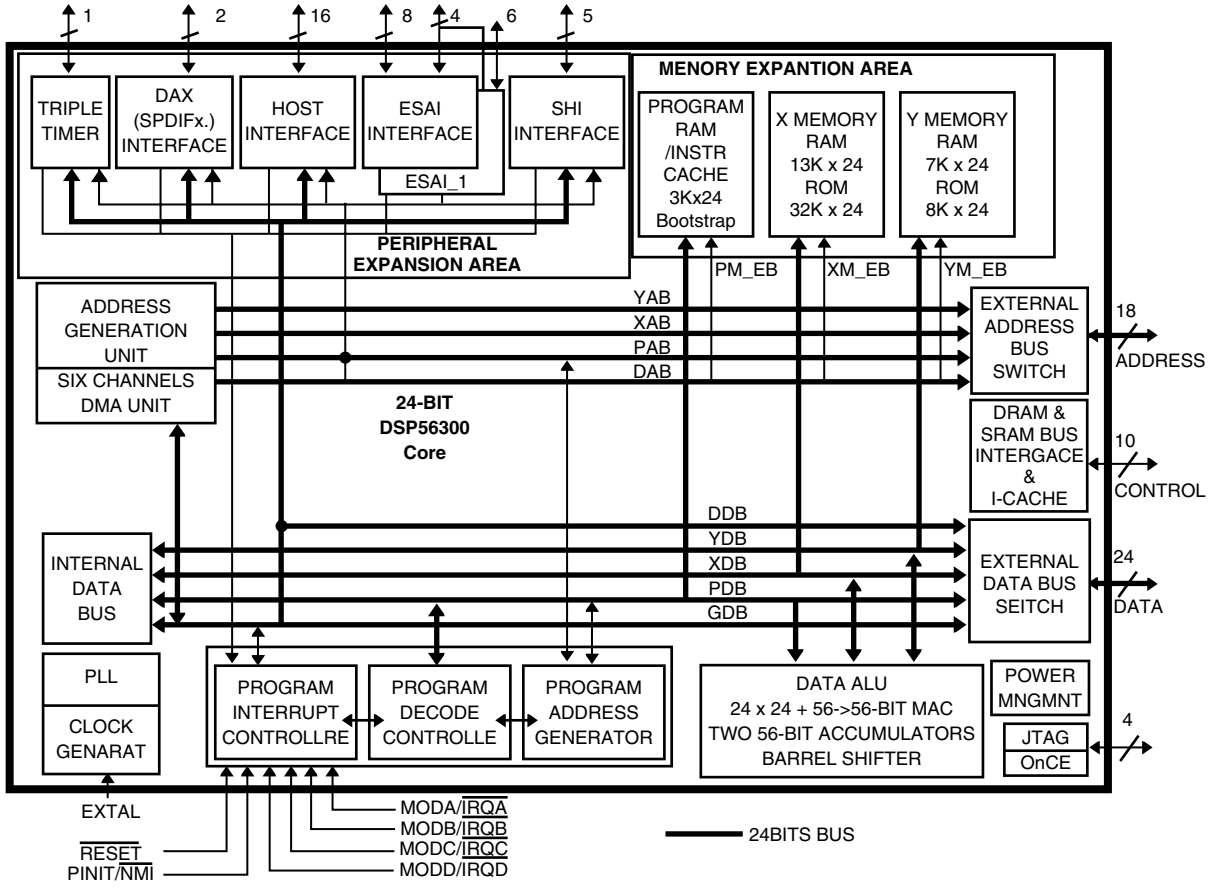
I=CMOS, I1=Schmitt, Ip2=Schmitt with pull-down resistor, O=CMOS (H=VDD, L=VSS)

## ■XCA56367PV150 (IC661, IC666) : DSP

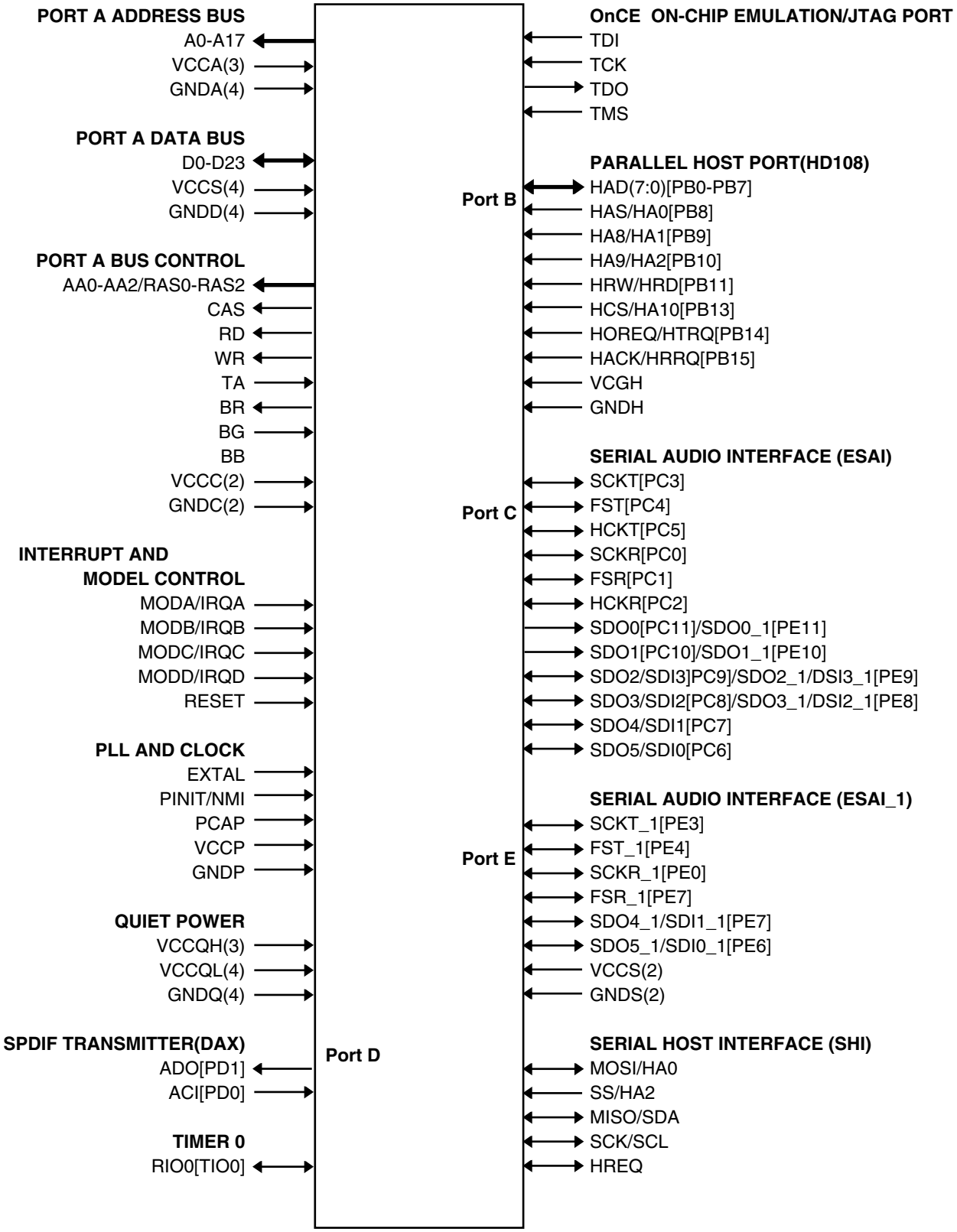
1. Pin layout




2. Block diagram

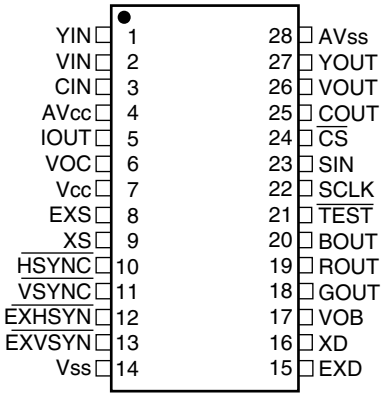


3. Signal groupings



## ■MB90088 (IC403) : Screen display controller

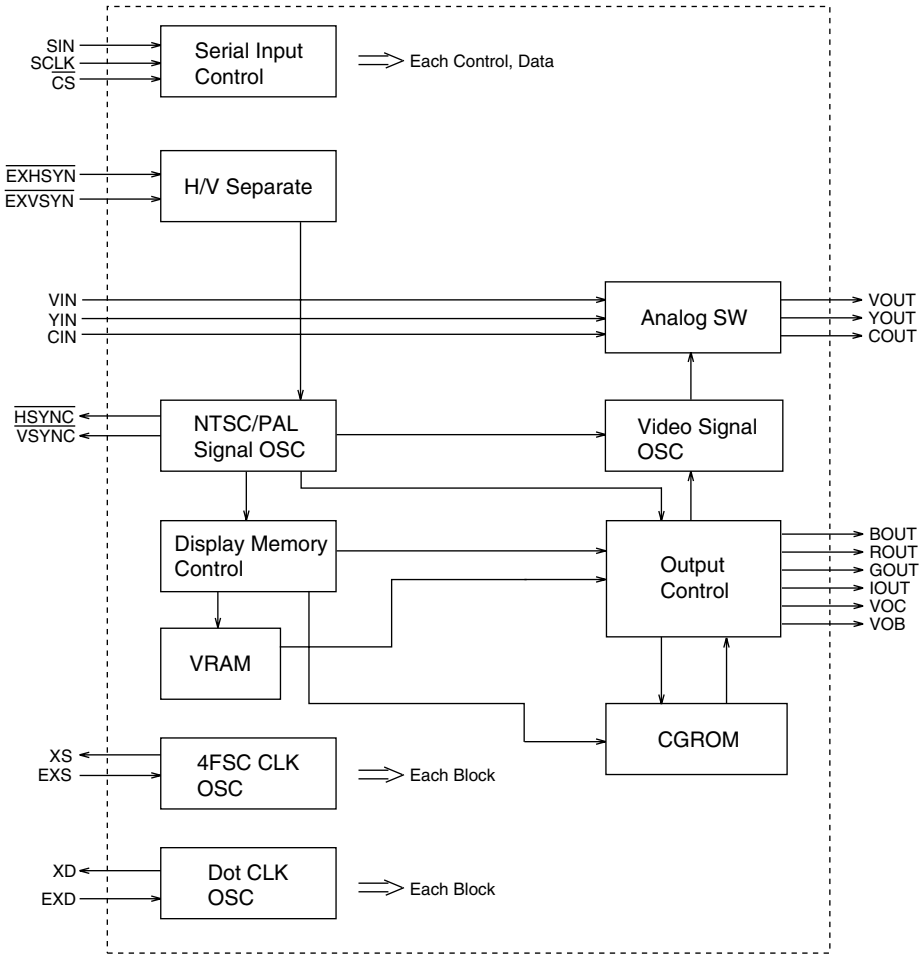
1. Pin layout



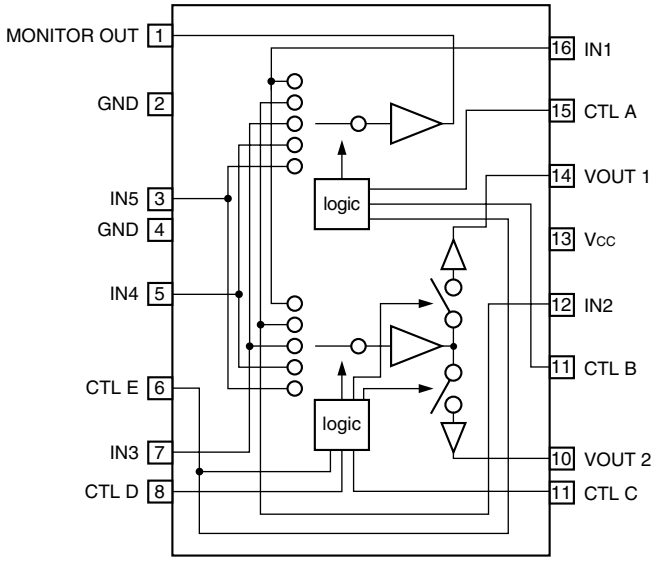

2.Pin functions

| Pin No. | Symbol | I/O | Function |
|---|---|---|---|
| 1 | YIN | I | Lux signal Input terminal for Superinpause indication |
| 2 | VIN | I | Composite video signal input terminal for Superinpause indication |
| 3 | CIN | I | Contrast signal input terminal for Superinpause indication |
| 4 | AVcc | - | Analog power supply terminal |
| 5 | IOUT | O | Color (Lux) signal output terminal |
| 6 | VOC | O | Character output terminal |
| 7 | Vcc | - | Power supply terminal |
| 8 | EXS | I | Clock generater outside circuit terminal for color burst |
| 9 | XS | O | |
| 10 | HSYNC | O | Horizontal signal output terminal |
| 11 | VSYNC | O | Vertical signal output terminal |
| 12 | EXHSYN | I | EXT horizontal signal input terminal |
| 13 | EXVSYN | I | EXT vertical signal input terminal |
| 14 | Vss | - | GND |
| 15 | EXD | I | Dot clock generater outside circuit signal terminal for indication |
| 16 | XD | O | |
| 17 | VOB | O | Character & background signal output terminal |
| 18 | GOUT | O | Color signal (Green, Red, Blue) |
| 19 | ROUT | | |
| 20 | BOUT | | |
| 21 | TEST | I | Test signal input terminal |
| 22 | SCLK | I | Shift clock input terminal for serial transmission |
| 23 | SIN | I | Serial data input terminal |
| 24 | CS | I | Chip select terminal |
| 25 | COUT | O | Contrast signal output terminal |
| 26 | VOUT | O | Composite video signal output terminal |
| 27 | YOUT | O | Lux signal output terminal |
| 28 | AVss | - | Analog GND terminal |

3.Block diagram



## ■ BA7625 (IC401, IC431, IC451) : Video selector

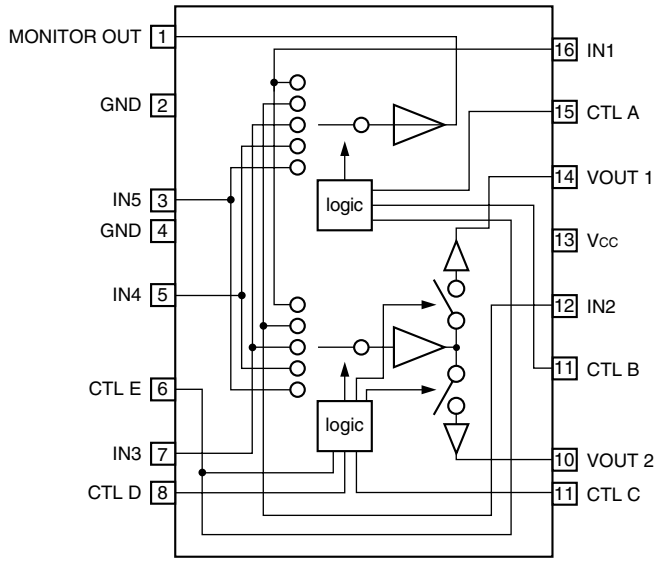



| A | B | E | MONITOR OUT |
|---|---|---|---|
| L | L | * | IN1 |
| H | L | * | IN2 |
| L | H | * | IN3 |
| H | H | L | IN4 |
| H | H | H | IN5 |

| C | D | E | VOUT1 |
|---|---|---|---|
| L | L | * | -- |
| H | L | * | IN2 |
| L | H | * | IN3 |
| H | H | L | IN4 |
| H | H | H | IN5 |

| C | D | E | VOUT2 |
|---|---|---|---|
| L | L | * | IN1 |
| H | L | * | -- |
| L | H | * | IN3 |
| H | H | L | IN4 |
| H | H | H | IN5 |

## ■ BA7626 (IC732) : Video selector

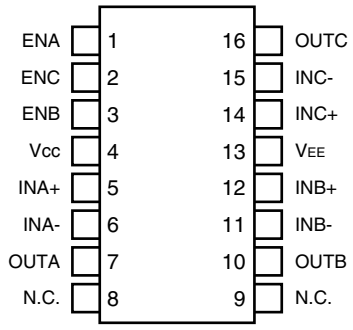



| A | B | E | MONITOR OUT |
|---|---|---|---|
| L | L | * | IN1 |
| H | L | * | IN2 |
| L | H | * | IN3 |
| H | H | L | IN4 |
| H | H | H | IN5 |

| C | D | E | VOUT1 |
|---|---|---|---|
| L | L | * | -- |
| H | L | * | IN2 |
| L | H | * | IN3 |
| H | H | L | IN4 |
| H | H | H | IN5 |

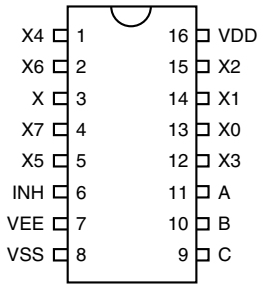
| C | D | E | VOUT2 |
|---|---|---|---|
| L | L | * | IN1 |
| H | L | * | -- |
| L | H | * | IN3 |
| H | H | L | IN4 |
| H | H | H | IN5 |

## ■ MAX4018ESD (IC503, IC544) : Op. amp.

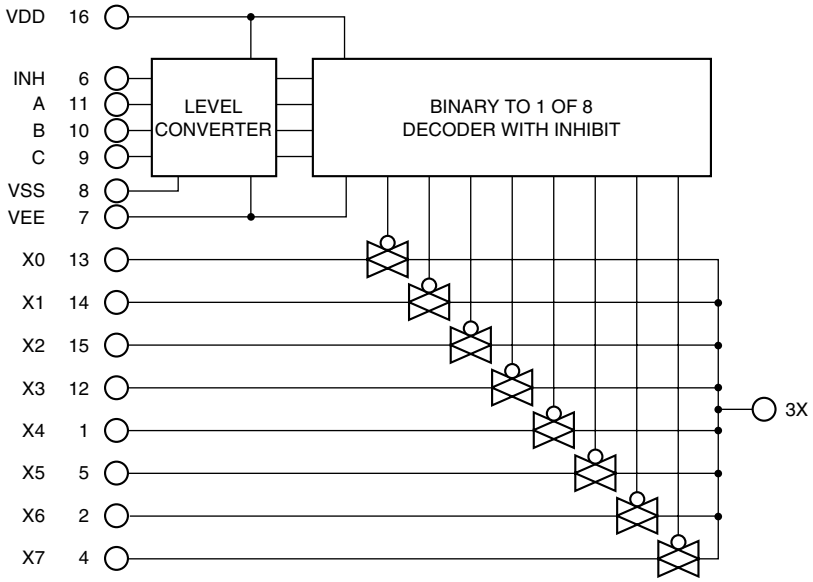


## ■ BU4051BC (IC461) : Analog multiprexers/ DE multiprexers

1. Pin layout

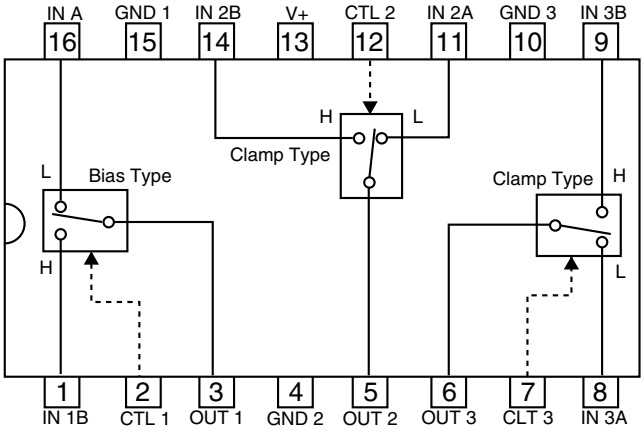



2.Brock Diagram

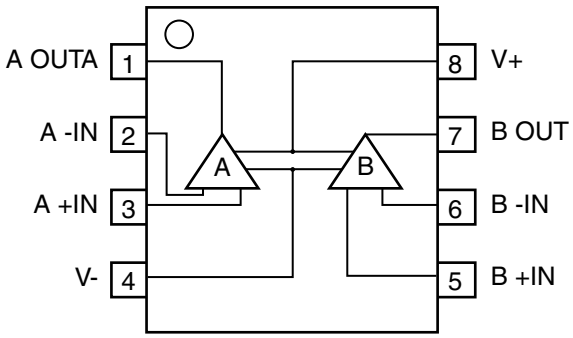



## ■ NJM2285V (IC402) : Video switch

1. Blick diagram



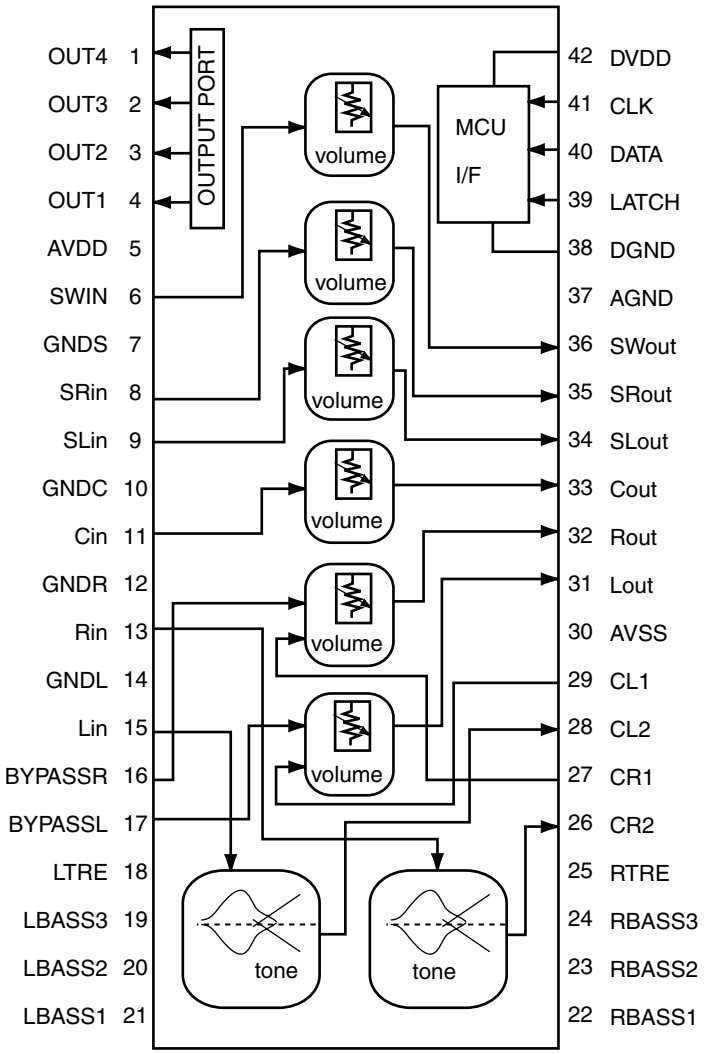

## ■ NJM4580E (IC201, 204, 241, 242, 251, 252, 253, 254, 271, 272, 273, 281, 631, 632, 633, 636, 637, 638, 641, 642, 643, 646, 647, 648, 655, 656, 686, 687) : L.P.F.




(TOP VIEW)

## ■ M62446FP (IC653) : 6CH master volume

1.Block Diagram

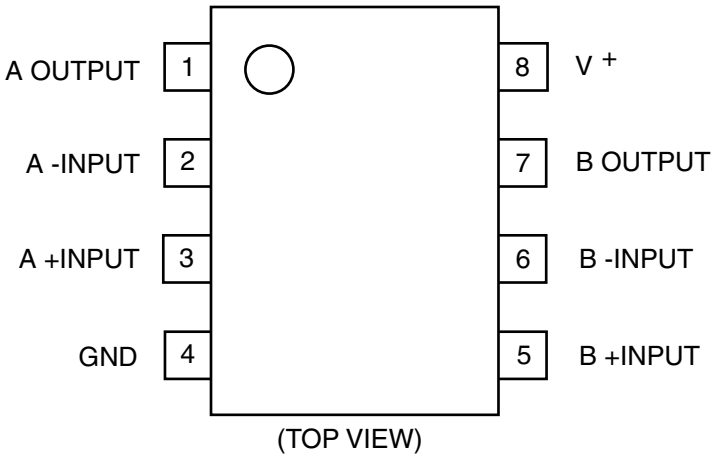



2. Pin functions

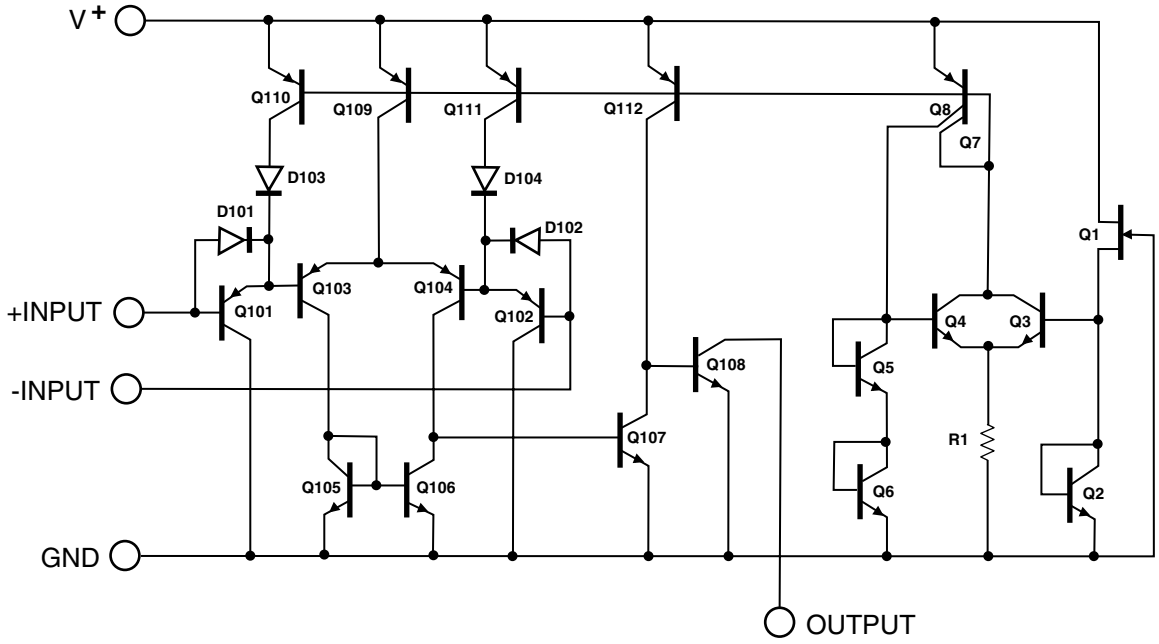
| Pin No. | Symbol | I/O | Descriptions |
|---|---|---|---|
| 1 | SURROUND | O | SURROUND control terminal |
| 2 | BASS BOOST | O | BASS BOOST control terminal |
| 3 | INPUT-ATT | O | Input attenuator control terminal |
| 4 | MUTING | O | MUTING control terminal |
| 5 | AVDD | - | Analog positive power supply terminal |
| 6 | SWIN | I | SUB Woofer volume signal input terminal |
| 7 | A.GND | - | Analog ground terminal |
| 8 | RR IN | I | R ch volume signal input terminal for rear speaker |
| 9 | RL IN | I | L ch volume signal input terminal for rear speaker |
| 10 | A.GND | - | Analog ground terminal |
| 11 | C IN | I | Center volume signal input terminal |
| 12 | A.GND | - | Analog ground terminal |
| 13 | R IN | I | R ch volume signal input terminal |
| 14 | A.GND | - | Analog ground terminal |
| 15 | L IN | I | L ch volume signal input terminal |
| 16,17 | | - | Non connect |
| 18 | | - | Frequency adjustment terminal tone/treble |
| 19~21 | | - | Frequency adjustment terminal tone/bass |
| 22 | | O | Tone output terminal |
| 23,24 | | - | Frequency adjustment terminal tone/bass |
| 25 | | - | Frequency adjustment terminal tone/treble |
| 26 | | - | Frequency adjustment terminal tone/bass |
| 27 | | I | L/R volume input terminal |
| 28 | | O | Tone output terminal |
| 29 | | I | L/R volume input terminal |
| 30 | AVSS | - | Analog negative power supply terminal |
| 31 | L OUT | O | L ch output |
| 32 | R OUT | O | R ch output |
| 33 | C OUT | O | Center volume signal output terminal |
| 34 | RL OUT | O | L ch volume signal output terminal for rear speaker |
| 35 | RR OUT | O | R ch volume signal output terminal for rear speaker |
| 36 | SW OUT | O | SUB Woofer volume signal output terminal |
| 37 | A.GND | - | Analog ground terminal |
| 38 | D.GND | - | Digital ground terminal |
| 39 | VOL STB | I | Latch input terminal |
| 40 | VOL DATA | I | Volume data input terminal |
| 41 | VOL CLK | I | Clock input terminal for data transfer |
| 42 | DVDD | - | Digital power supply terminal |

## ■ NJM2903M (IC282, IC998) : Temperature detector

1. Pin layout

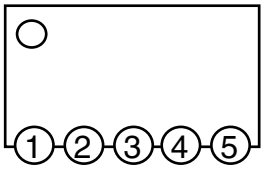



2. Block diagram

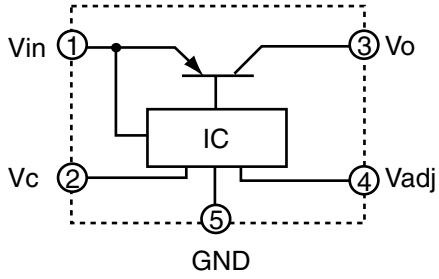



## ■ PQ20VZ11 (IC690) : Reguratpr

1.Pin layout

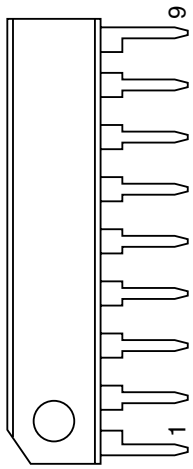



2.Block daigram

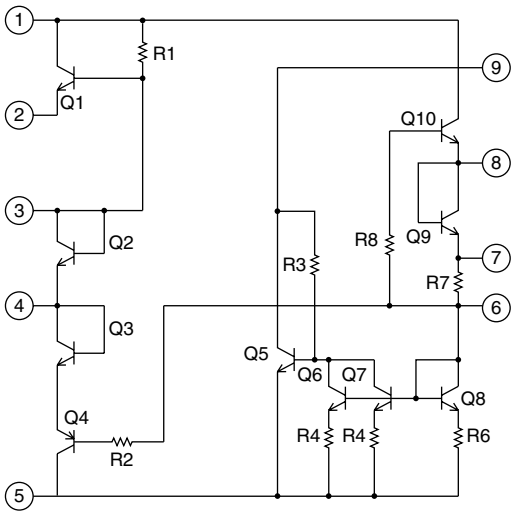


## ■ VC5022-2 (IC601, IC603, IC605, IC606, IC607) : Advanced super A

1. Pin layout

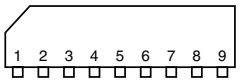



2. Block diagram

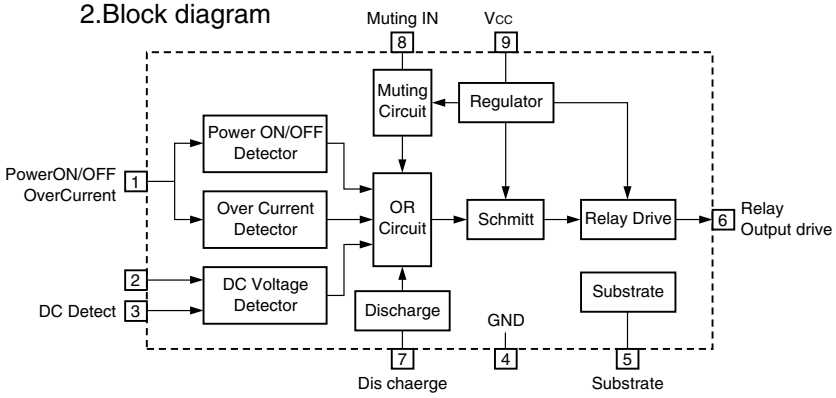



## ■TA7317P (IC951) : Protecter

1.Pin layout

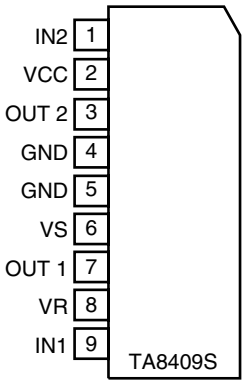



2.Block diagram




## ■ TA8409S (IC967) : Motor driver

1.Pin layout



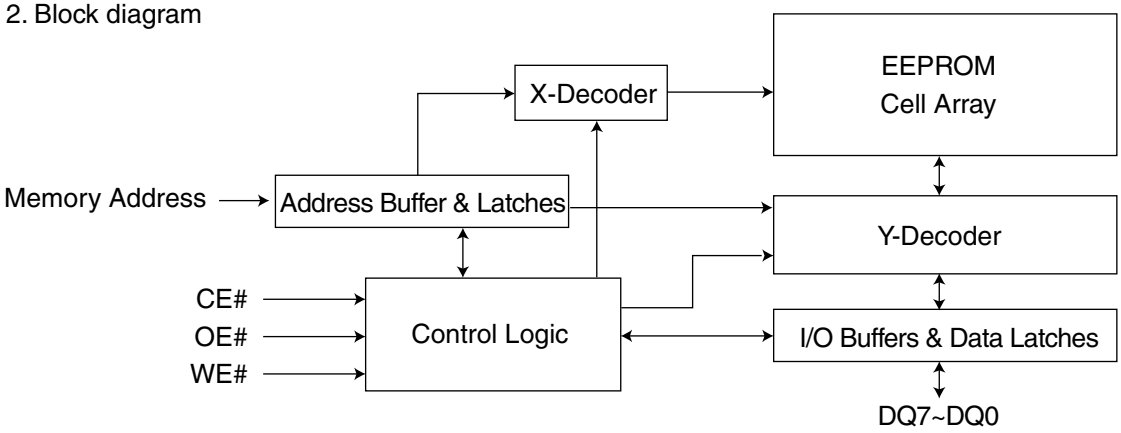

2.Pin function

| INPUT | | OUTPUT | | MODE |
|---|---|---|---|---|
| IN1 | IN2 | OUT1 | OUT2 | MOTOR |
| 0 | 0 | ∞ | ∞ | STOP |
| 1 | 0 | H | L | CW/CCW |
| 0 | 1 | L | H | CCW/CW |
| 1 | 1 | L | L | BRAKE |

## ■ SST39VF010-7CWH (IC667) : EEPROM

1. Pin layout

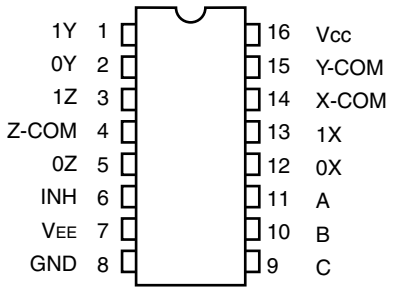

2. Block diagram




3. Pin function

| Symbol | Pin name | Function |
|---|---|---|
| AMS- A0 | Address Inputs | To provide memory address. During Sector-Erase AMS-A12 address lines will select the sector. |
| DQ7- DQ0 | Data Input/Output | To output data during read cycles and receive input data during write cycles. Data is internally latched during a write cycle. The outputs are in tri-state when OE# or CE# is high. |
| CE# | Chip Enable | To active the device when CE# is low. |
| OE# | Output Enable | To gate the data output buffers. |
| WE# | Write Enable | To control the write operations. |
| VDD | Power Supply | To provide power supply voltage: 3.0-3.6V for SST39LF512/010/020/040<br>2.7-3.6V for SST39VF512/010/010/040 |
| Vss | Ground | |
| NC | No Connection | Unconnected Pins |

## ■ TC74HC4053AF (IC501, IC502, IC541, IC542, IC543) : Multiplexer

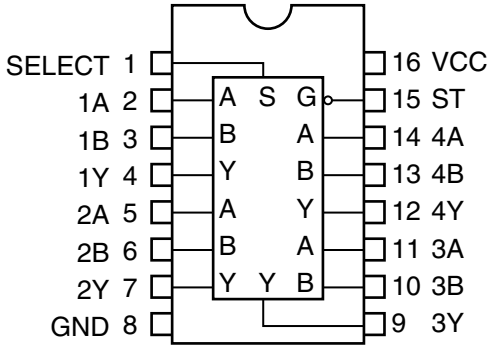



| CONTROL INPUTS | | | | "ON" CHANNEL |
|---|---|---|---|---|
| INHIBIT | C | B | A | |
| L | L | L | L | 0X, 0Y, 0Z |
| L | L | L | H | 1X, 0Y, 0Z |
| L | L | H | L | 0X, 1Y, 0Z |
| L | L | H | H | 1X, 1Y, 0Z |
| L | H | L | L | 0X, 0Y, 1Z |
| L | H | L | H | 1X, 0Y, 1Z |
| L | H | H | L | 0X, 1Y, 1Z |
| L | H | H | H | 1X, 1Y, 1Z |
| H | X | X | X | NONE |

X: Don't Care.

## ■ TC74VHC157FT (IC676, IC681, IC682) : Multiplexer

1. Pin layout



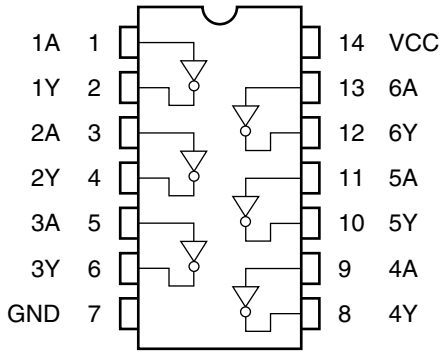

2. Truth table

| INPUT | | | | OUTPUT |
|---|---|---|---|---|
| ST | SELECT | A | B | |
| H | X | X | X | L |
| L | L | L | X | L |
| L | L | H | X | H |
| L | H | X | L | L |
| L | H | X | H | H |

X: Don't care

## ■ TC74HCT04AF (IC654) : Inverter

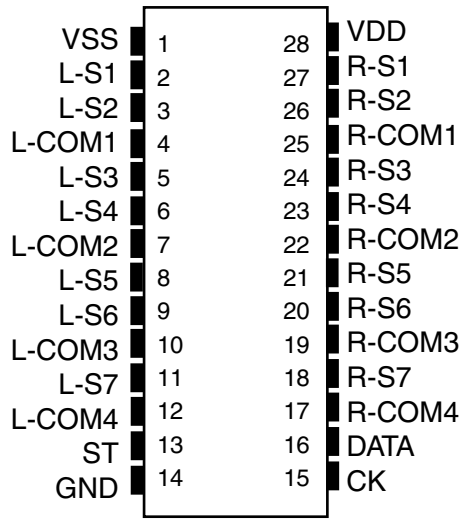
1. Pin layout

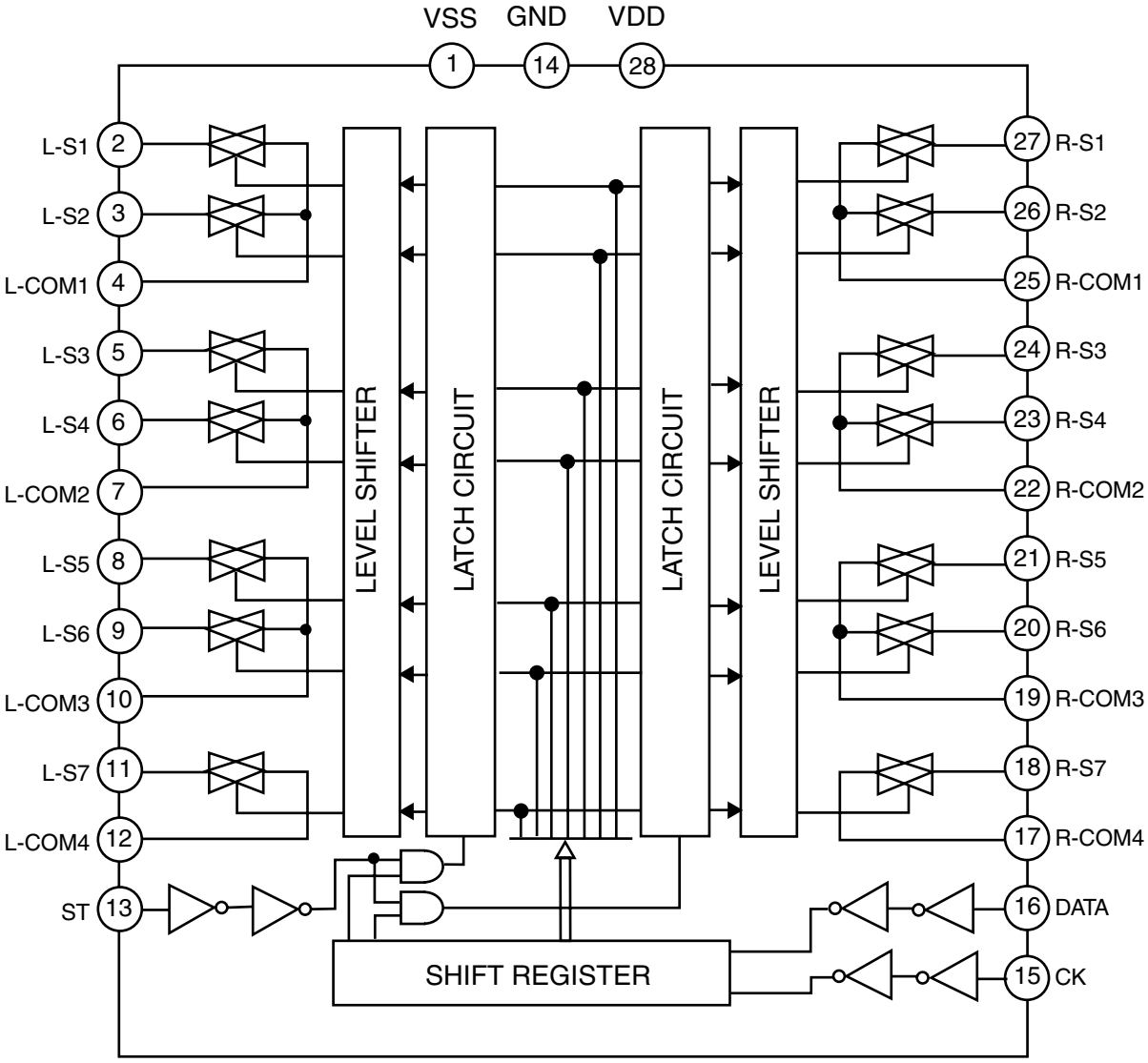



(TOP VIEW)

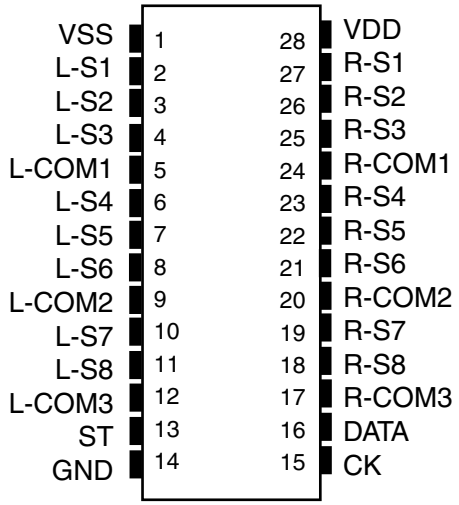
| A | Y |
|---|---|
| L | H |
| H | L |

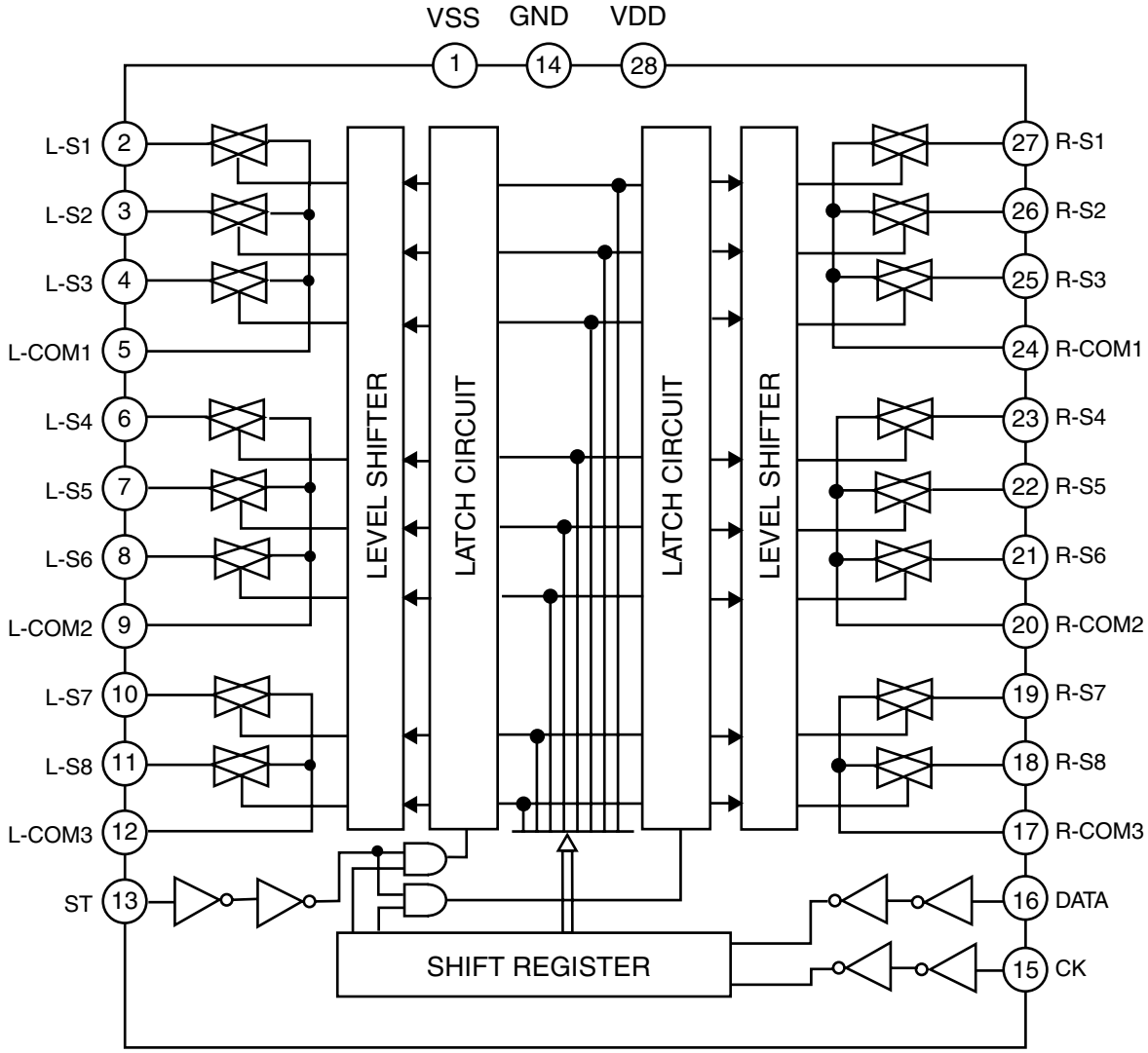
## ■ TC9162AF (IC211, IC213) : Analog switch



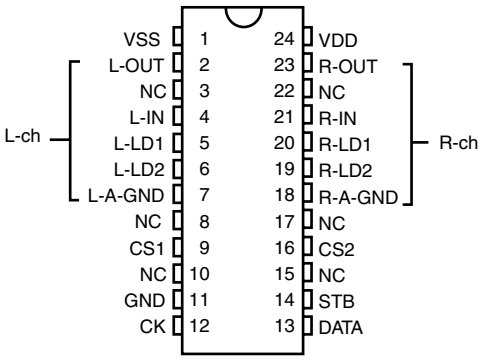
## ■TC9163AF (IC321) : Analog switch



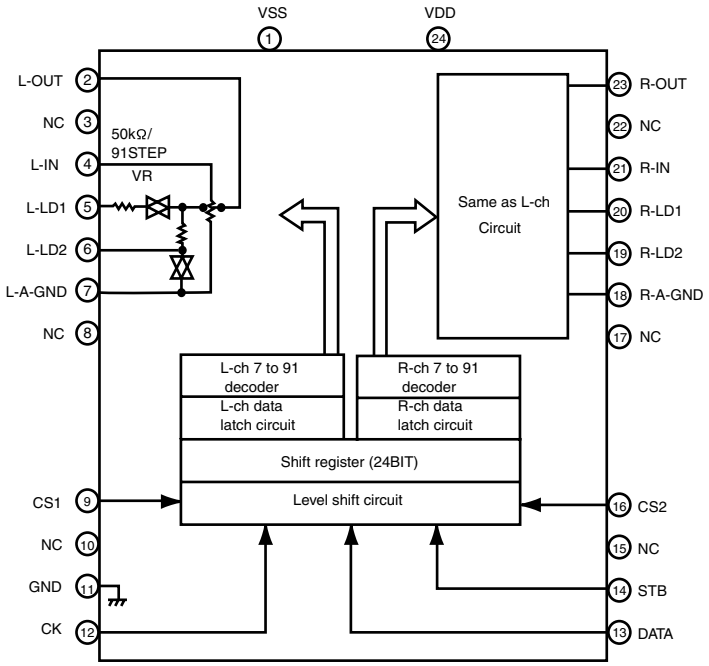



## ■ TC9459F (IC221, IC222, IC223, IC224) : Electronic volume control

1.Pin layout




2. Block diagram

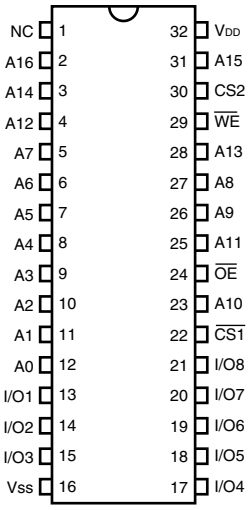



3.Pin function

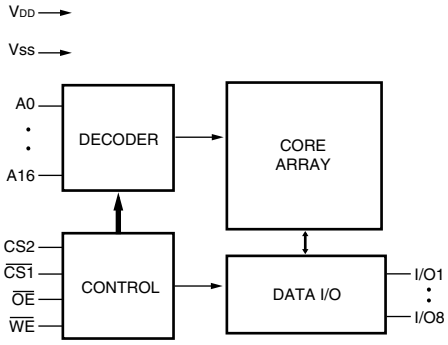
| Pin No. | Symbol | Function | Pin No. | Symbol | Function |
|---|---|---|---|---|---|
| 1 | VSS | Negative power supply pin | 13 | DATA | Data input pin |
| 2 | L-OUT | Volume output pin | 14 | STB | Strobe input pin |
| 3 | NC | No connection | 15 | NC | No connection |
| 4 | L-IN | Volume input pin | 16 | CS2 | Chip select input pin |
| 5 | L-LD1 | Loudness tap output pin | 17 | NC | No connection |
| 6 | L-LD2 | Loudness tap output pin | 18 | R-A-GND | Analog GND pin |
| 7 | L-A-GND | Analog GND pin | 19 | R-LD2 | Loudness tap output pin |
| 8 | NC | No connection | 20 | R-LD1 | Loudness tap output pin |
| 9 | CS1 | Chip select input pin | 21 | R-IN | Volume input pin |
| 10 | NC | No connection | 22 | NC | No connection |
| 11 | GND | Digital GND pin | 23 | R-OUT | Volume output pin |
| 12 | CK | Clock input pin | 24 | VDD | Positive power supply pin |

## ■ W24L010AJ-12 (IC668, IC669, IC670) : SRAM

1. Pin layout



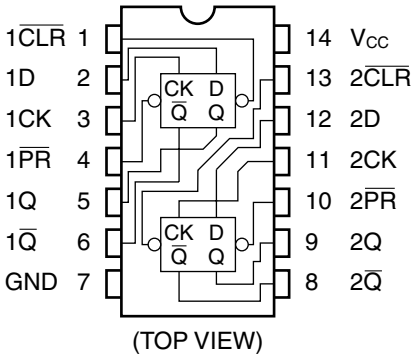

2. Block diaglam




3. Pin function

| SYMBOL | DESCRIPTION |
|---|---|
| A0 - A16 | Address Input |
| I/O1 - I/O8 | Data Input/Output |
| $\overline{CS1}$, CS2 | Chip Select Inputs |
| $\overline{WE}$ | Write Enable Input |
| $\overline{OE}$ | Output Enable Input |
| VDD | Power Supply |
| Vss | Ground |
| NC | No Connection |

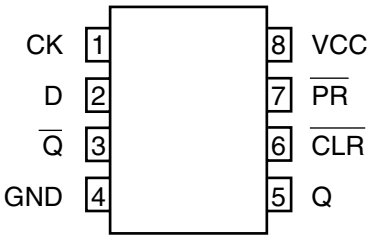
## ■ TC74VHC74FT (IC678, 683) : Flip-flop



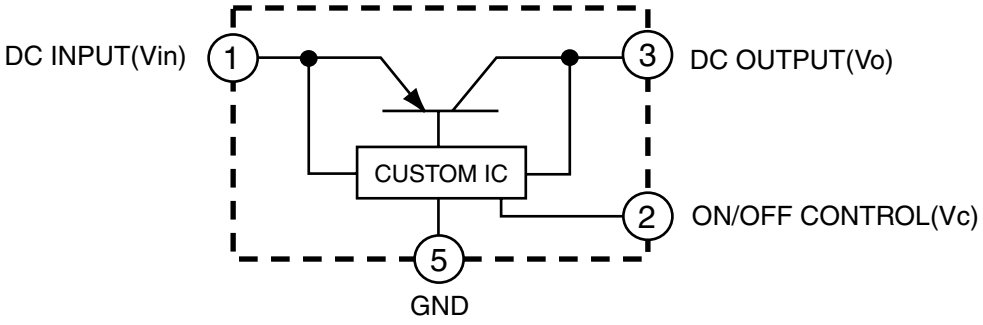

(TOP VIEW)

## ■ TC7WH74FU (IC659, 677) : Clock buffer

1. Pin layout




## ■ PQ3DZ53 (IC691, IC692, IC693, IC695) : Regulator



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